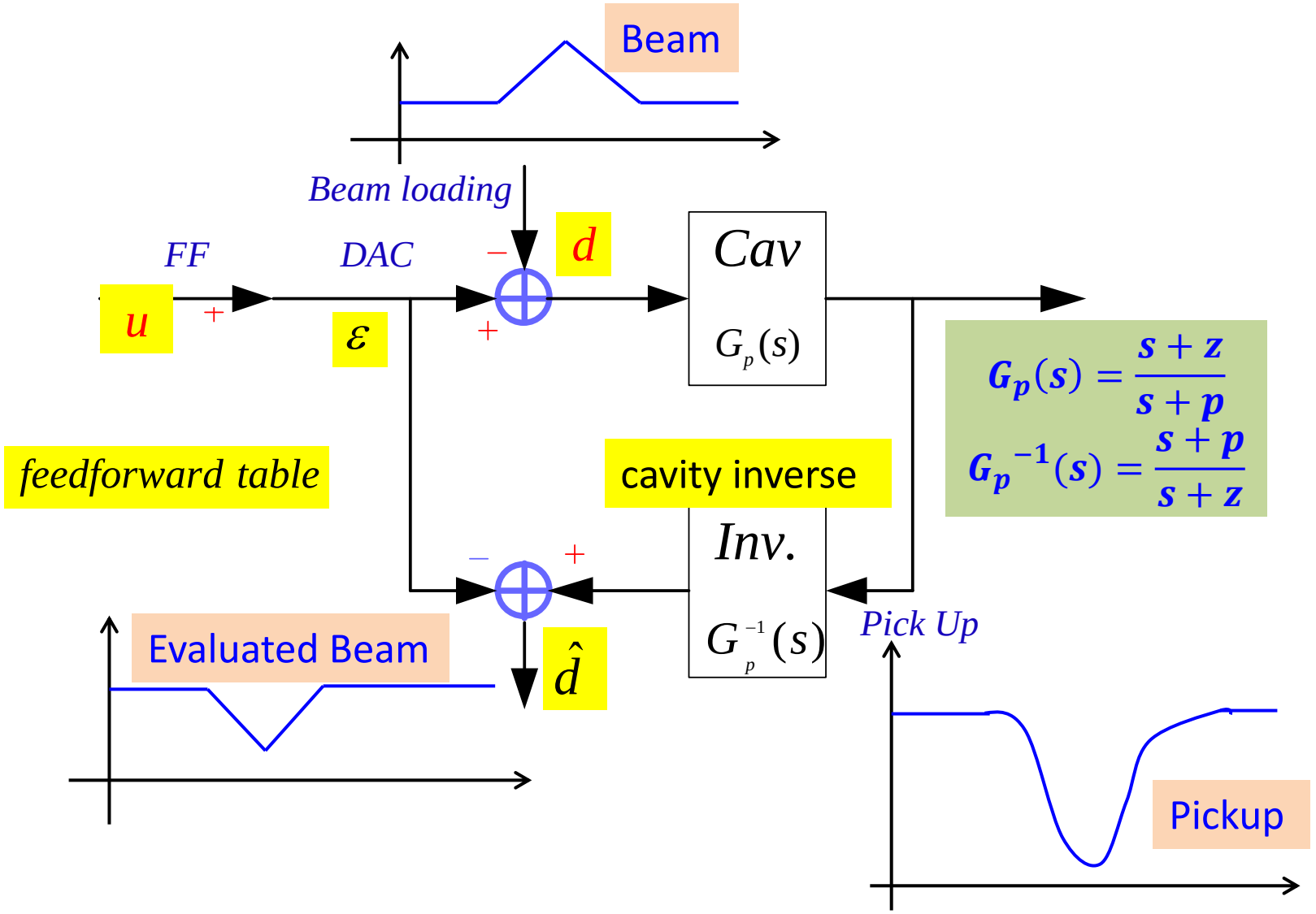
Model-based Controller

Feng QIU

Nov. 12, 2014 @ CERL (KEK)

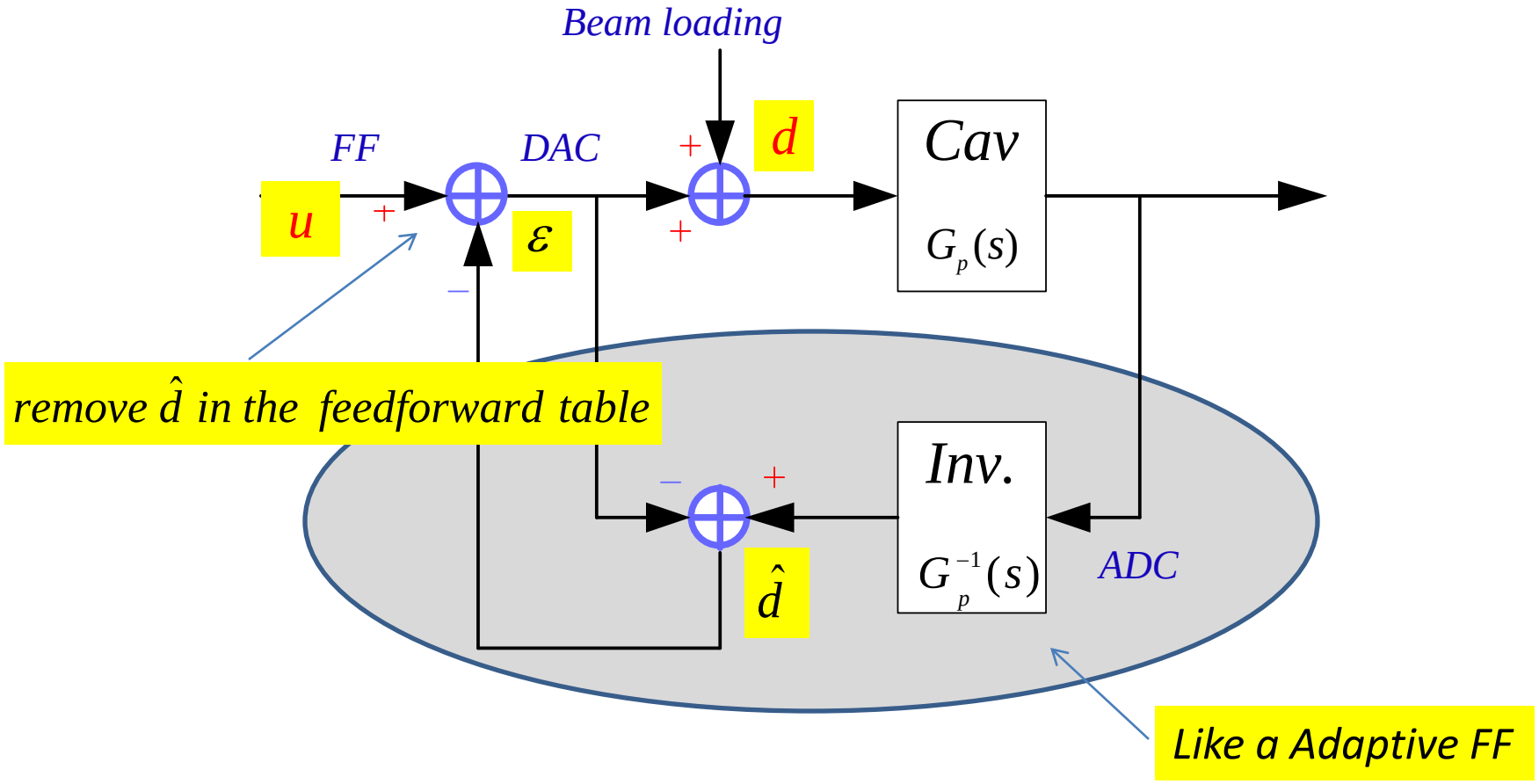
Model-based Applications

- What we can do if we "know" the system well?
- Can we evaluate the disturbing signal



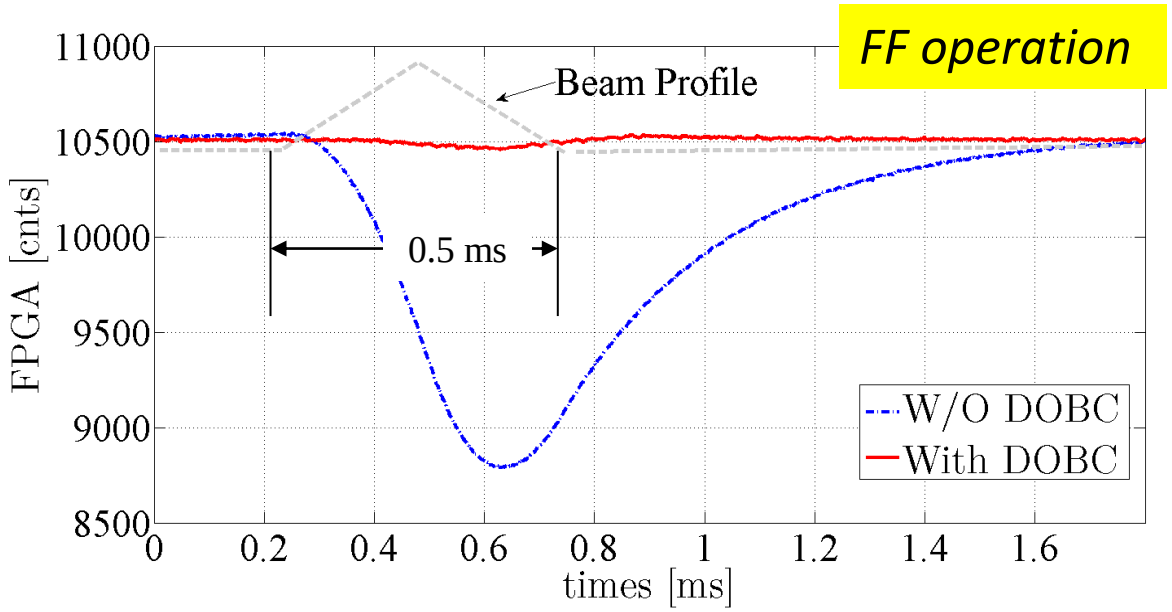
DOBC controller

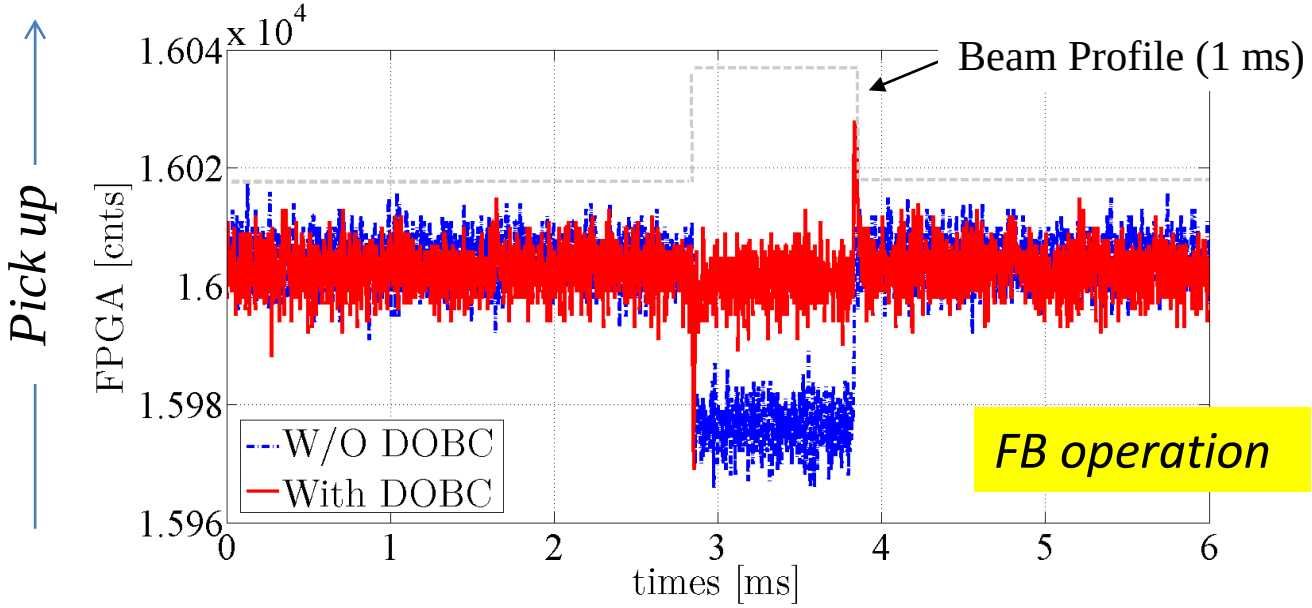
- Remove the evaluated disturbing signal $\hat{d}$ from FF table (seen beam loading as a external disturbance)
- This idea is named "Disturbance Observer-based Controller (DOBC)"



Preliminary results

- Primary experiment of this idea is implemented with cavity simulator (FPGA based).
- More discussion is necessary for detailed technology.





Thank you for your attention

Back up

First DOBC control in cERL LLRF system

Feng QIU

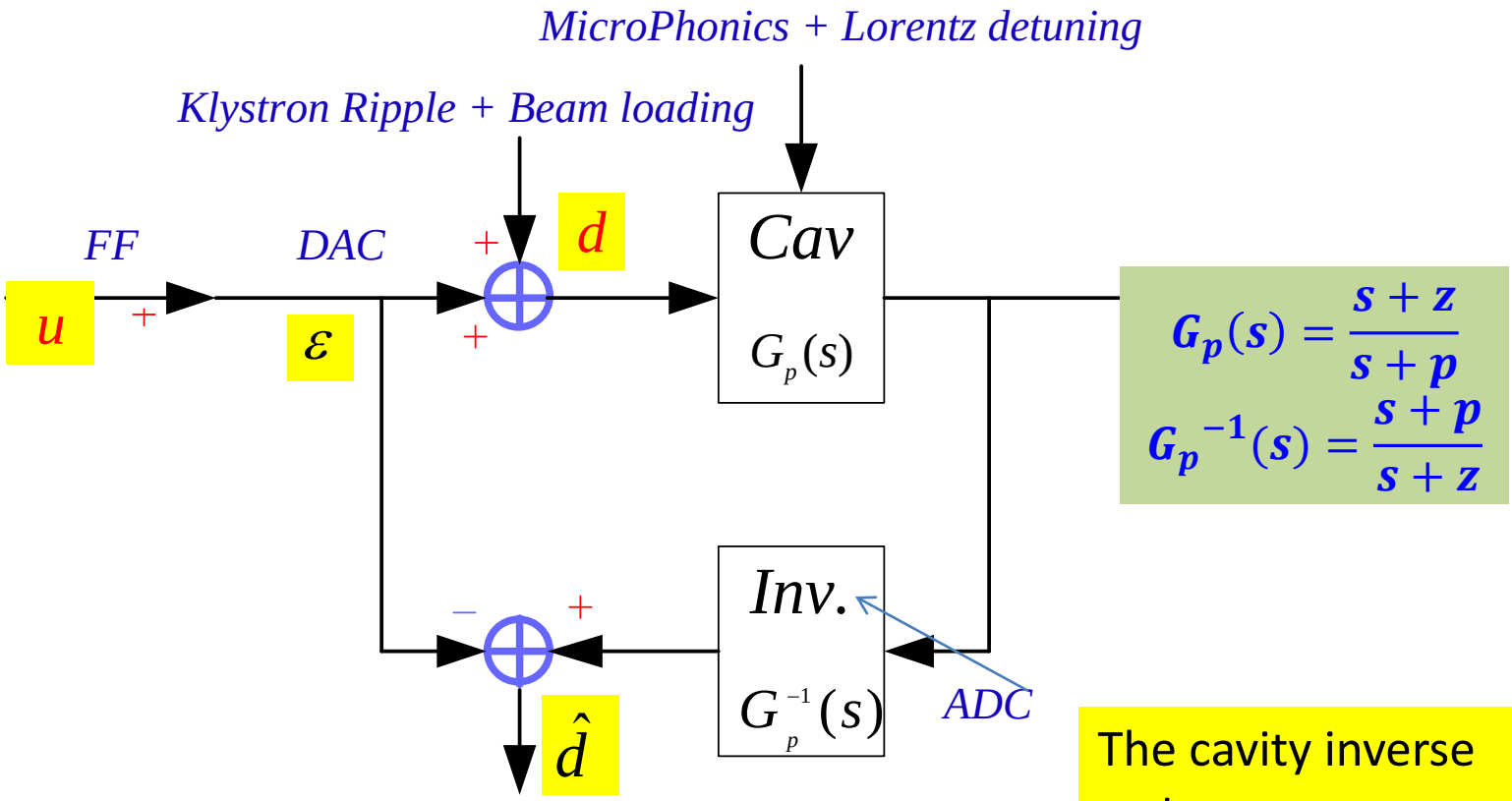
Oct. 20, 2014 @ CERL (KEK)

Main Content

- DOBC control (Review)
  I. Principle
  II. Simulation (PI vs. PI+DOBC)
- Programming (VHDL issue)
  I. Hardware Cost
- Test Bench (Cavity simulator + Controller)
- Result
  I. Square Beam
  II. Triangle Beam

DOBC control

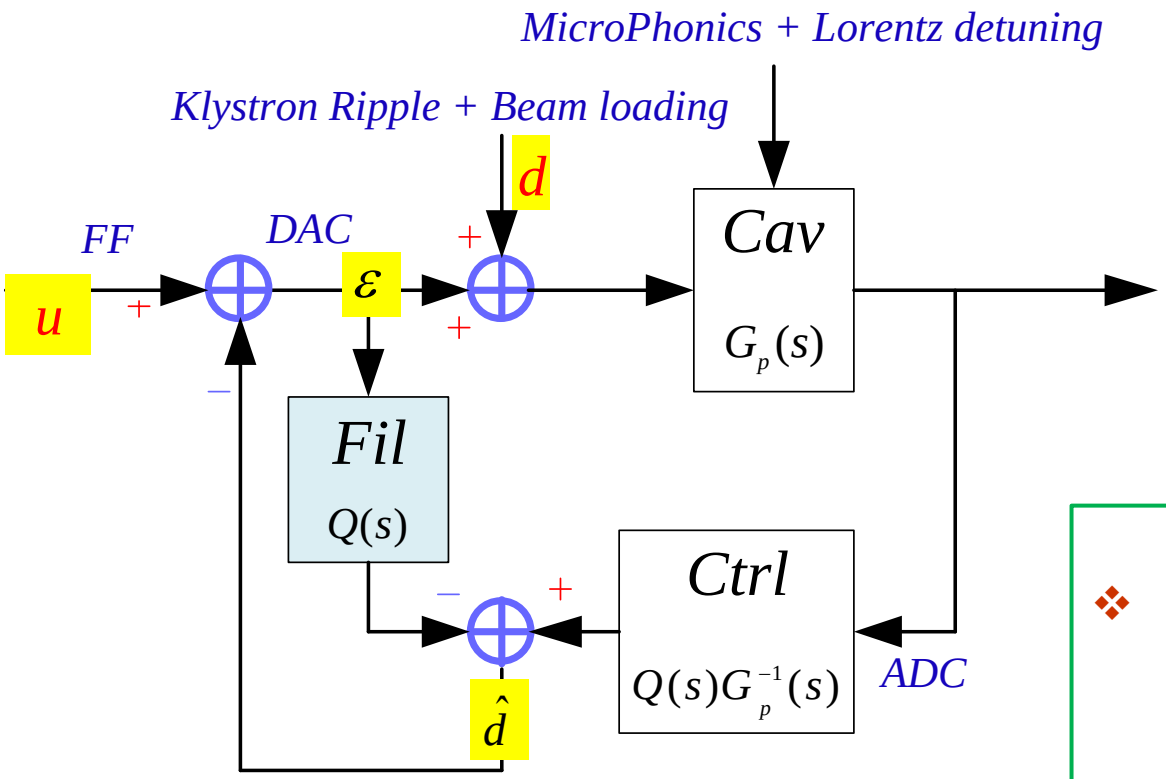
- What we can do if we "**know**" the system well?
- Can we evaluate the disturbing signal and remove them in the FF table?
- DOBC (**D**isturbance **OB**server **C**ontrol)



$$\hat{d} = (\varepsilon + d)G_p(s) \cdot G_P^{-1}(s) - \varepsilon = d$$

Model Based FB optimization

- The "Q" filter (LP filter) is used for improving the robustness (remove the high frequency noises)?



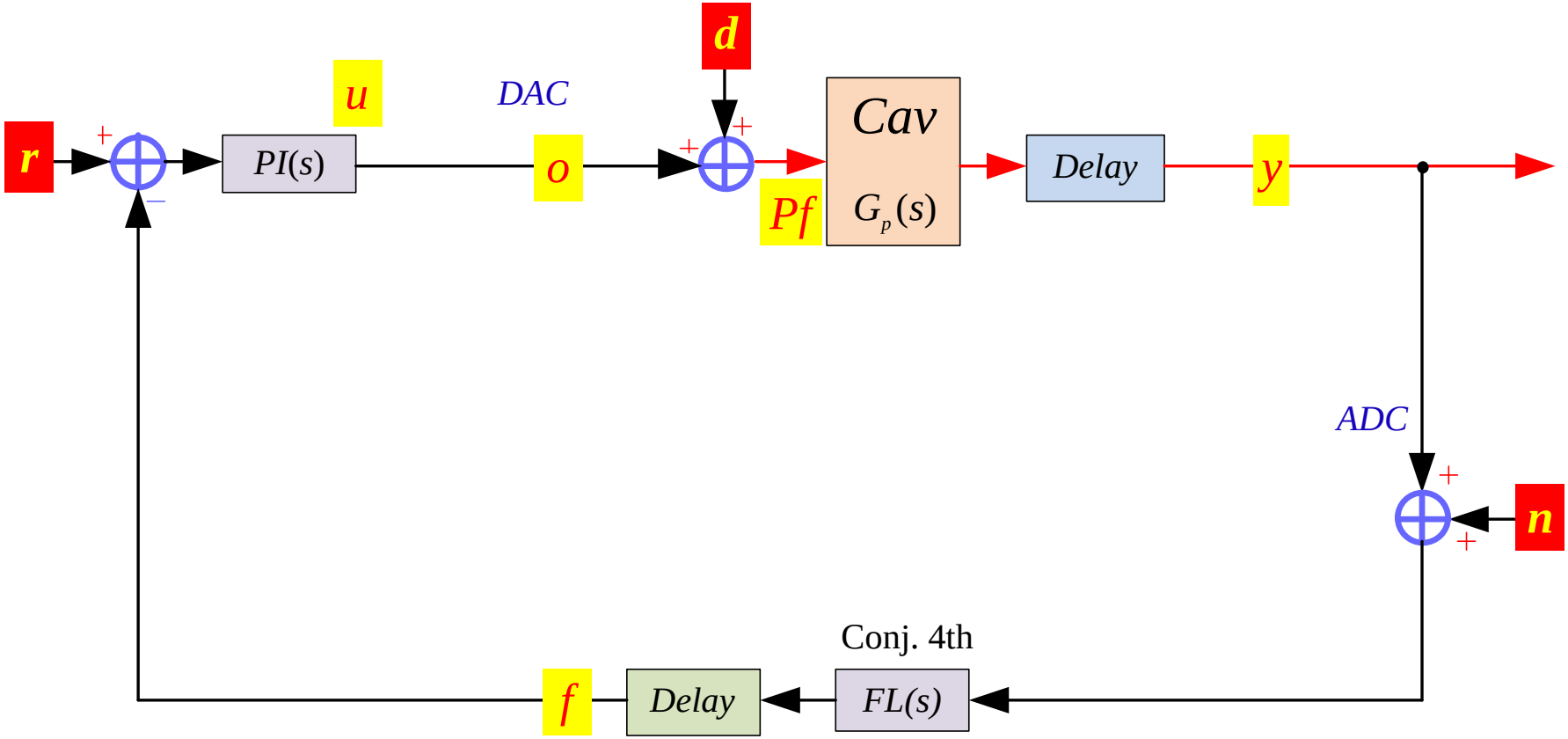
$$\hat{d} = (\varepsilon + d)G_p(s)\cdot G_P^{-1}(s)\cdot Q(s) - \varepsilon\cdot Q(s) = d\cdot Q(s)$$

Tips

- Connected another system $Q(s)$ with $G_P^{-1}(s)$ to make sure it can be physically realized.
- If the $Q(s)$ is an low-pass filter, then the d can be still evaluated.

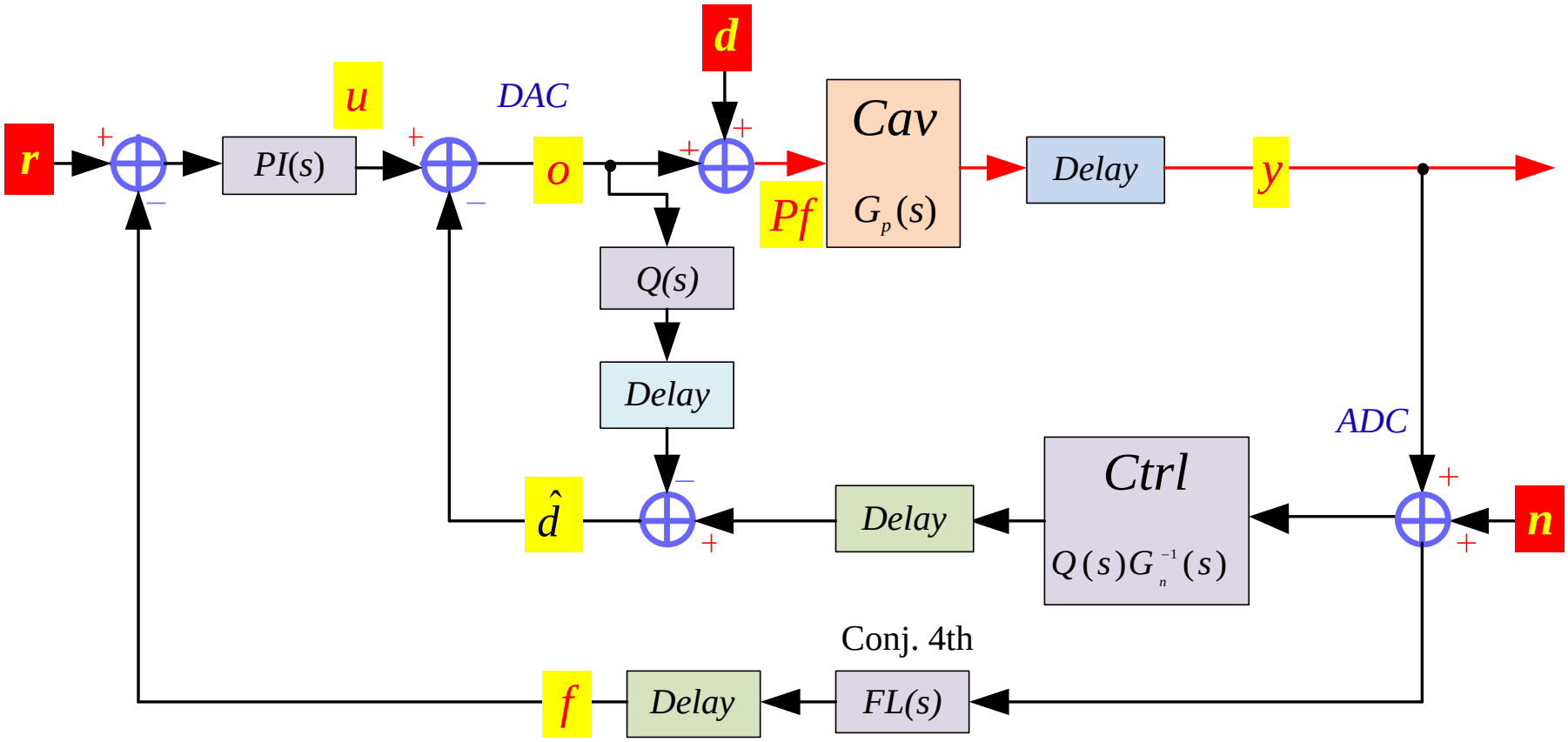
Traditional PI ctrl.

- PI Ctrl.



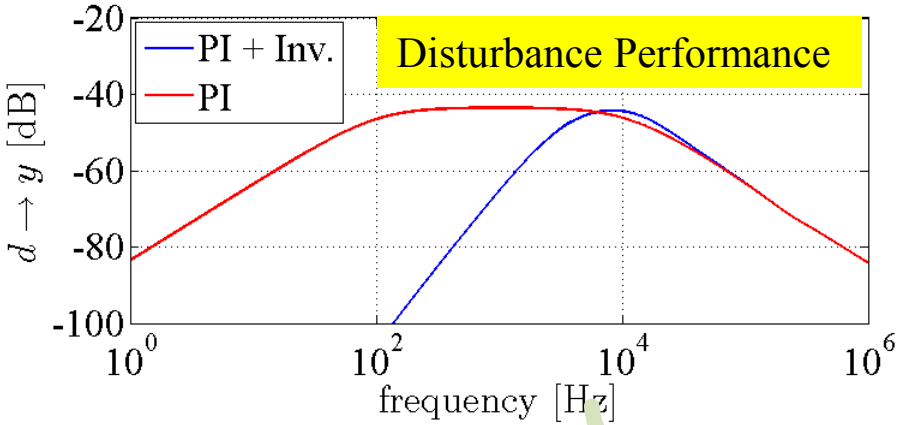
Total LLRF diagram

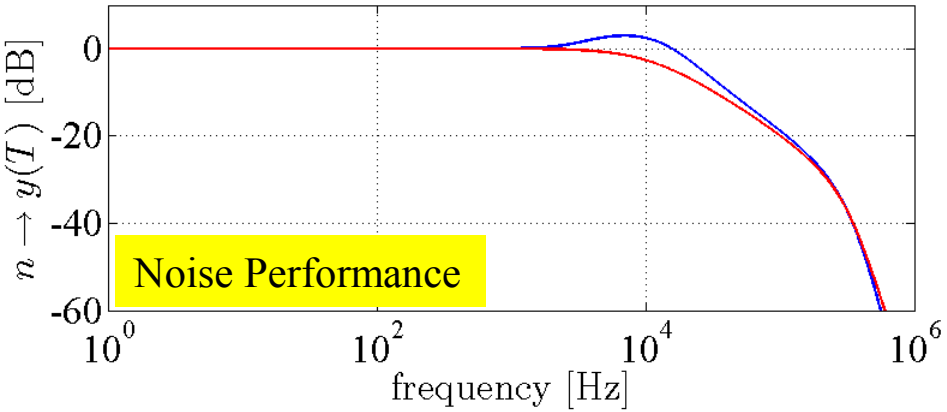
- PI + DOBC

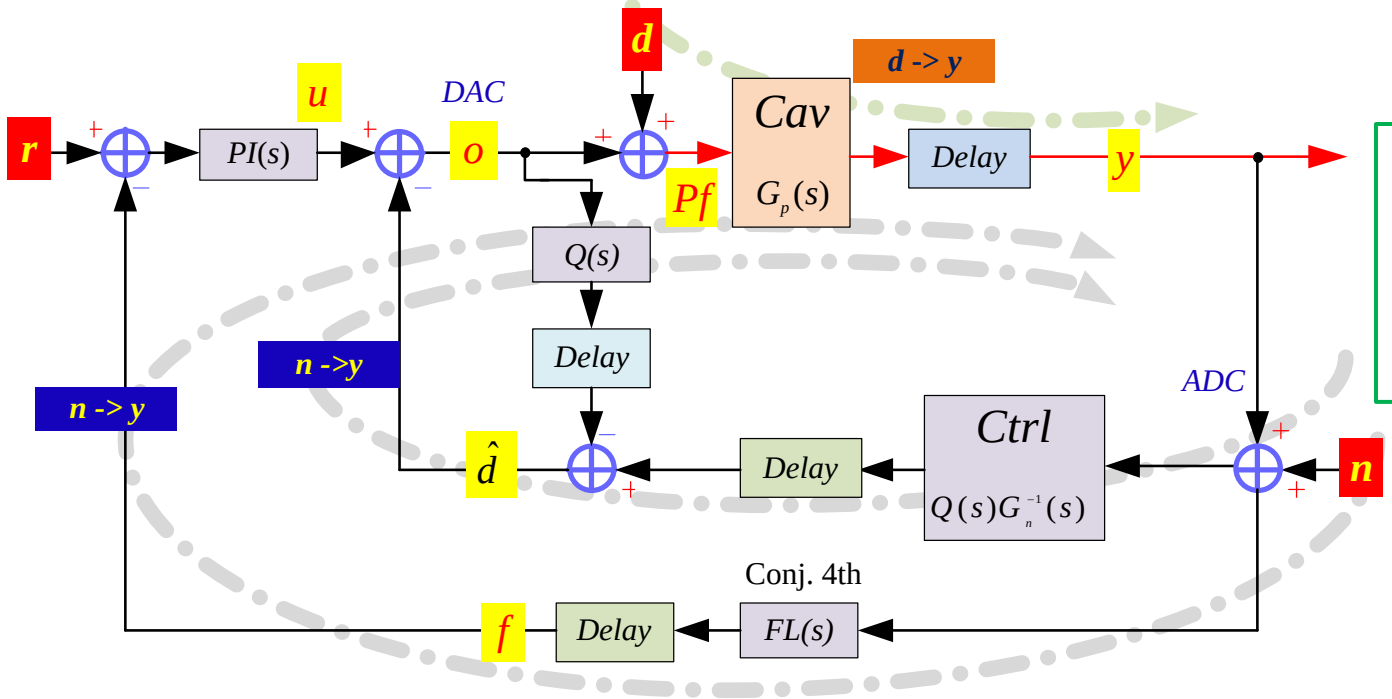


Comparison (Bode Diagram)

- PI Ctrl VS. PI+DOBC





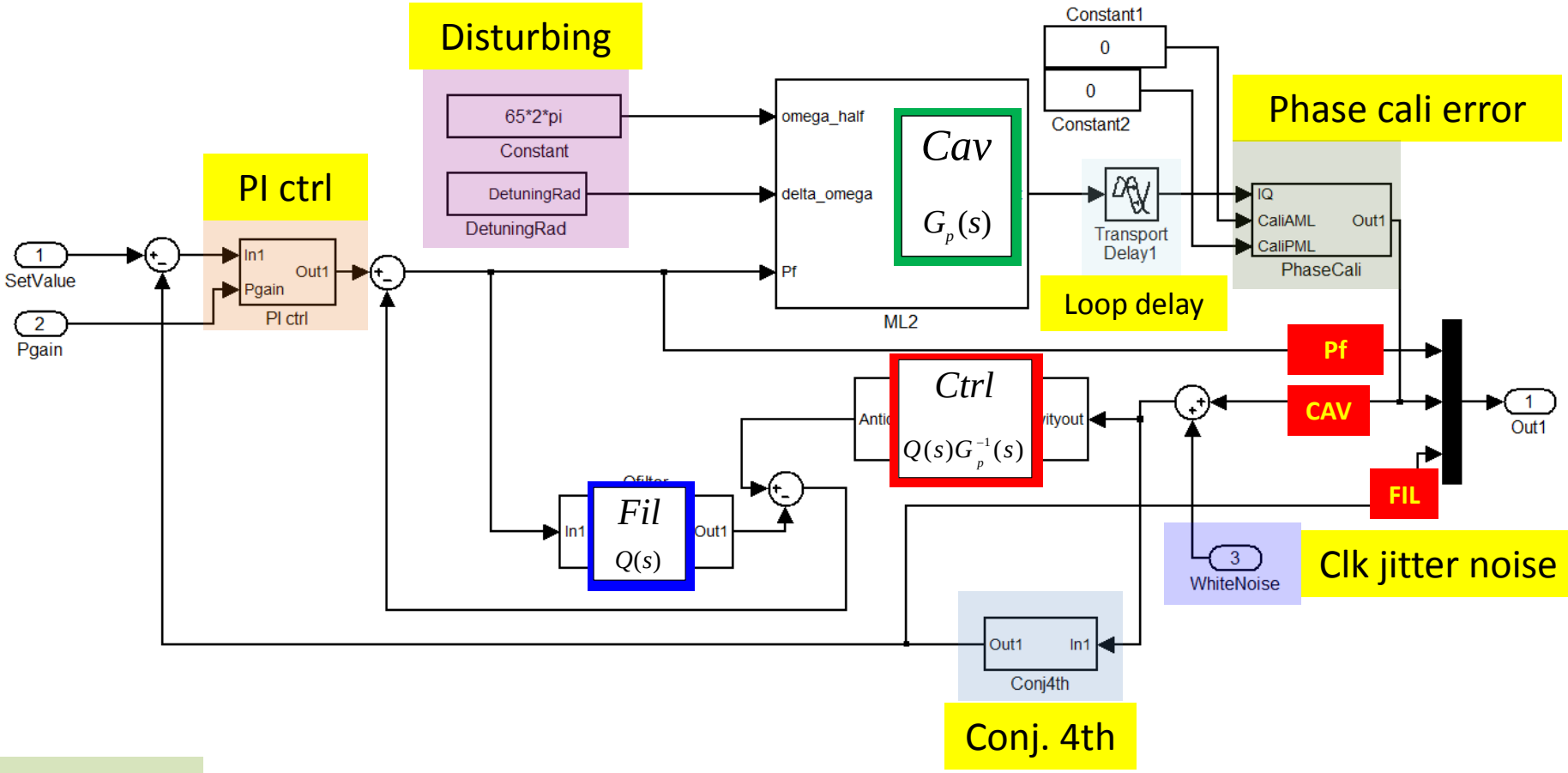


Tips

- Noise performance (worse)
- Disturbance performance (better)

Simulink Model

- Simulink Model (see AdvancedPIDV1.mdl)

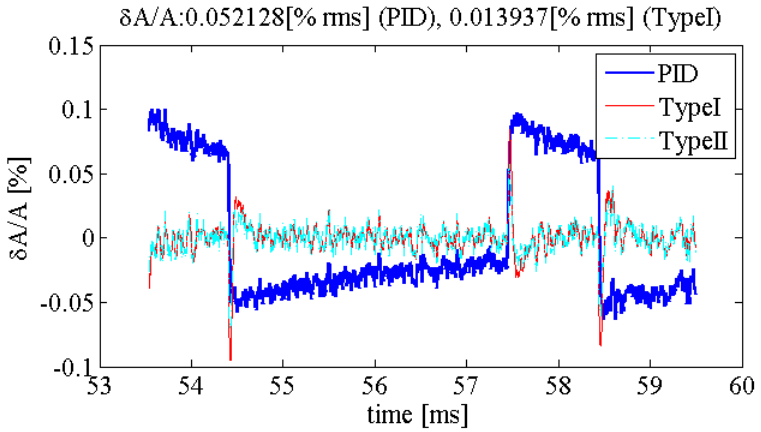


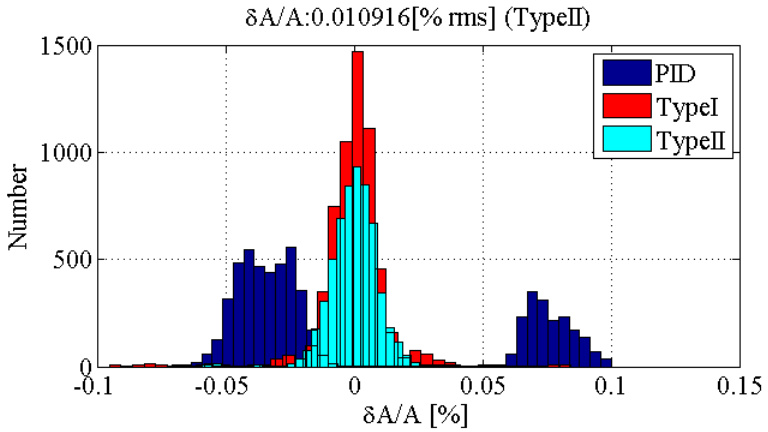
PI + DOBC

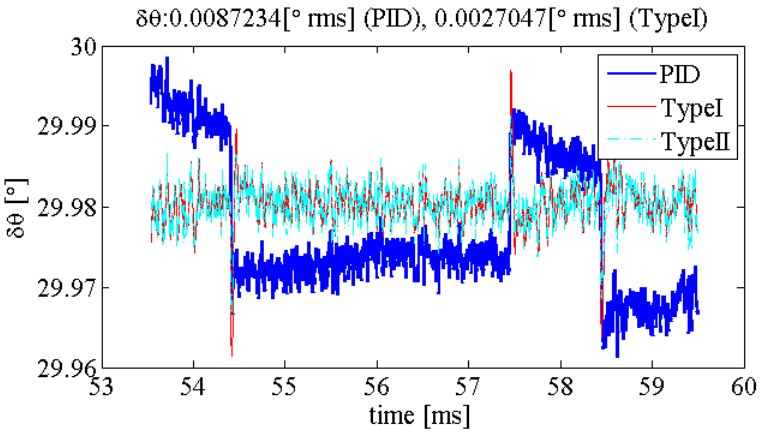
Simulation (Beam Loading compensation)

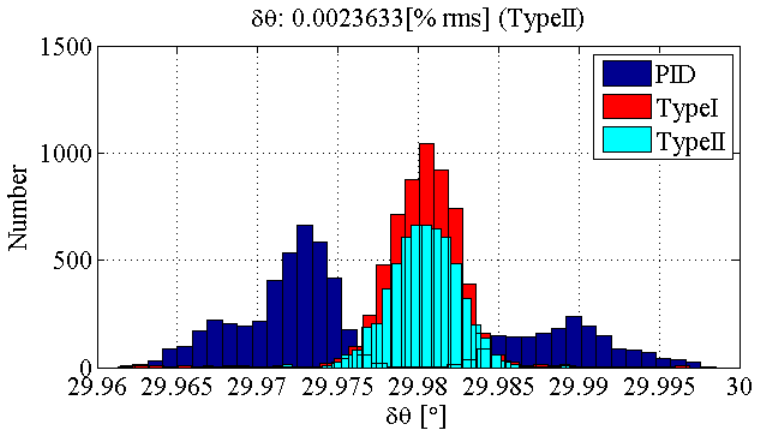
Beam Loading simulation

- Suppose worst beam loading (rectangle profile)
- Beam loading performance is better in DOBC control (TypeI and TypeII)









Programming (in theory)

FPGA Hardware Analysis					
Hardware		Grey Model (G)		BK model (G)	
		Q20	Q31	Q20	Q31
DSP48Es (Total 128 DSPs)	$Q - filter$	4	6	4	6
	$Q \cdot G^{-1}$	8	10	10	12
	I channel	12	16	14	18
	I/Q channel	24	32	28	36
Delays (1/81.25 MHz)	$Q - filter$	6	8	6	8
	$Q \cdot G^{-1}$	8	10	10	12

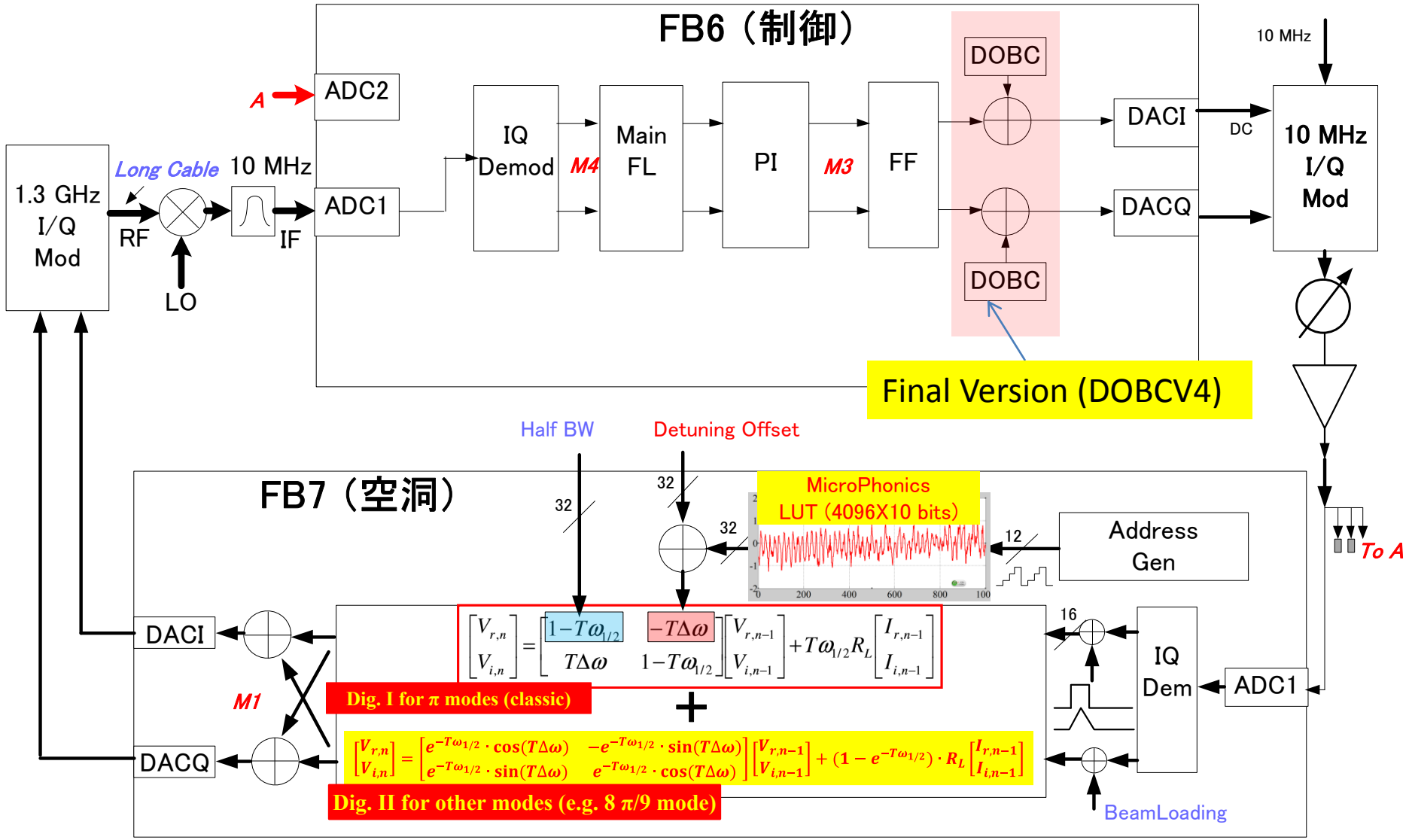
Second Order IIR filter

Programming (Real VHDL)

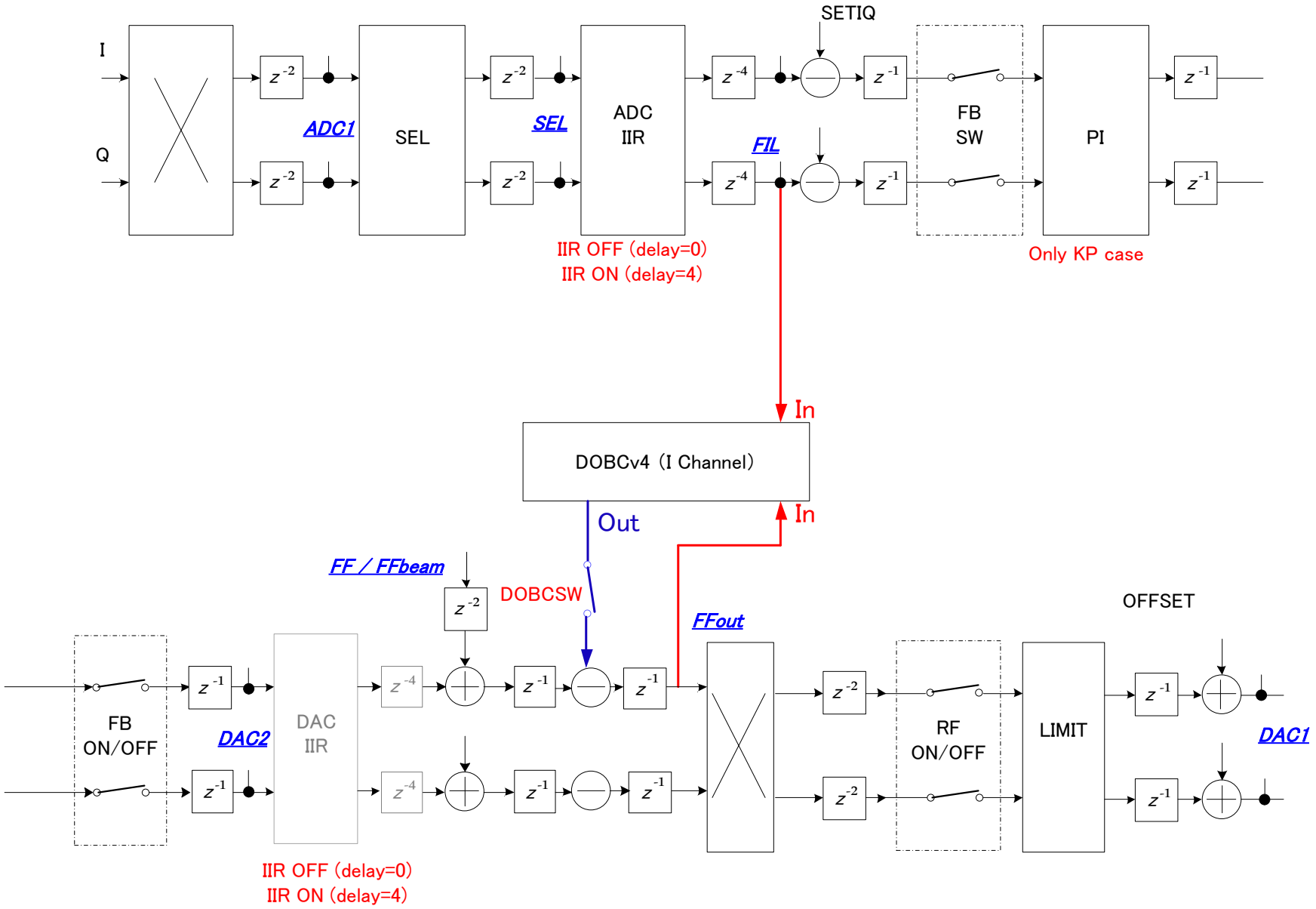
FPGA (Version)	DSP48Es (Total=128)	Timing Error
HO Low Pass	74	OK
HO Low Pass + Notch	84	OK
HO Low Pass + DOBC	104	NG (timing issue)
Conj.+1st Order + DOBC	92	OK

Final Version (DOBCV4)

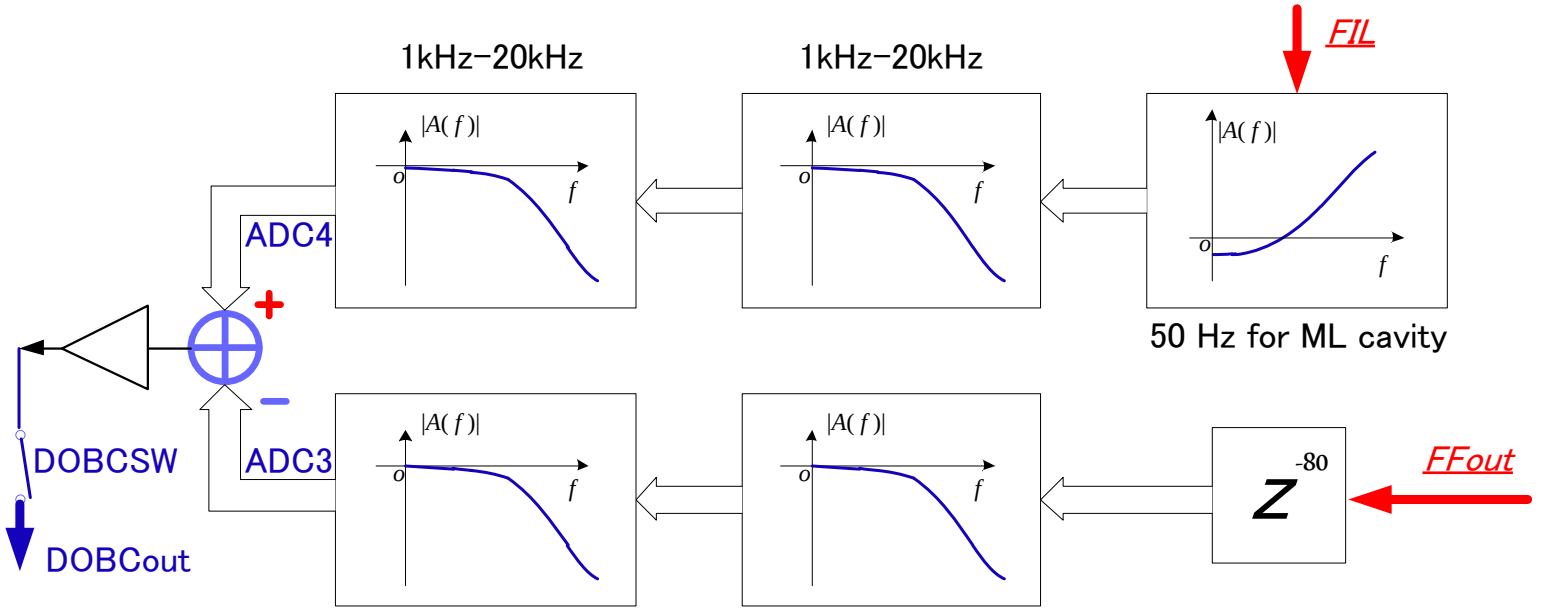
Test Bench (FB6 + FB7)



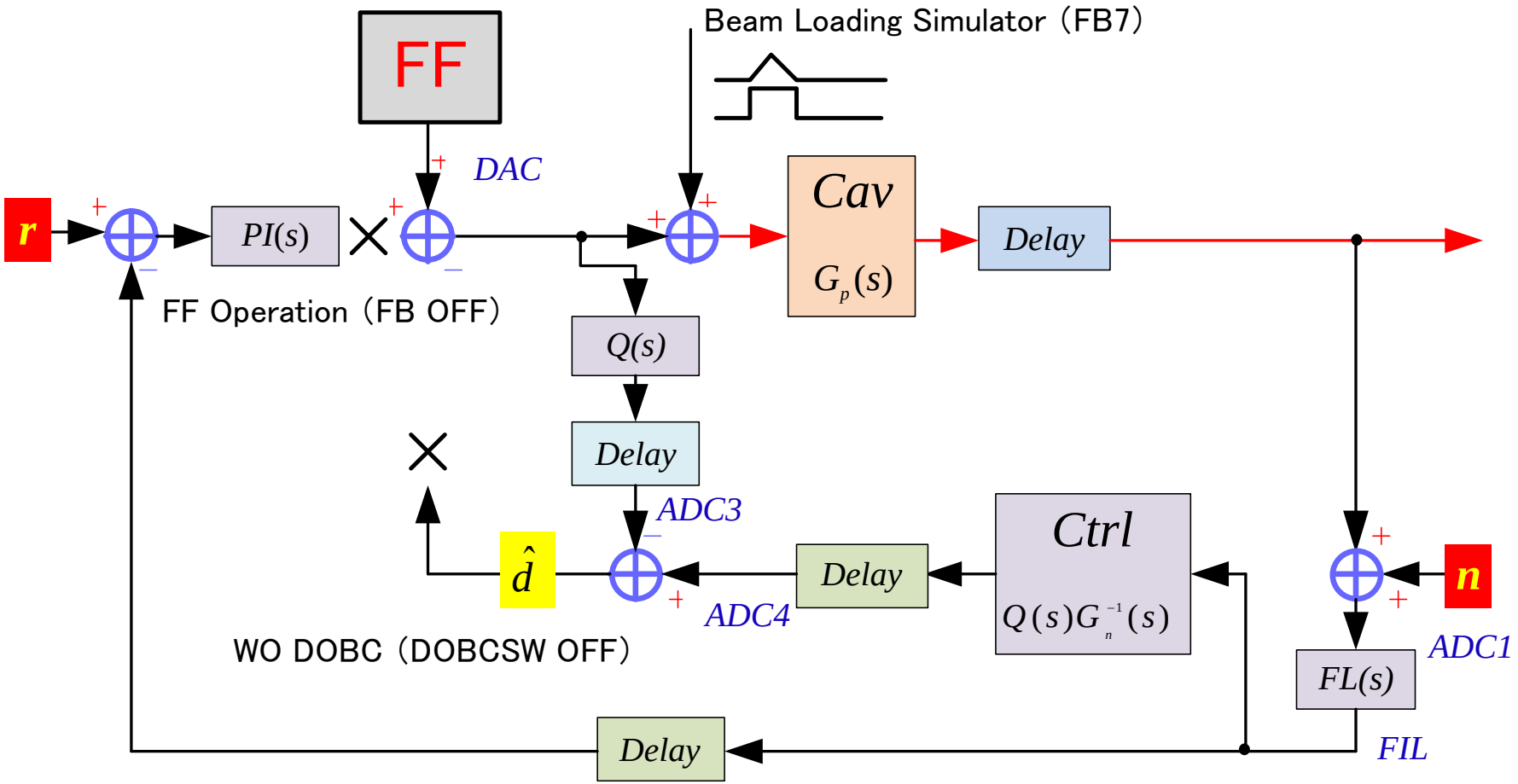
Algorithm（inside FPGA）



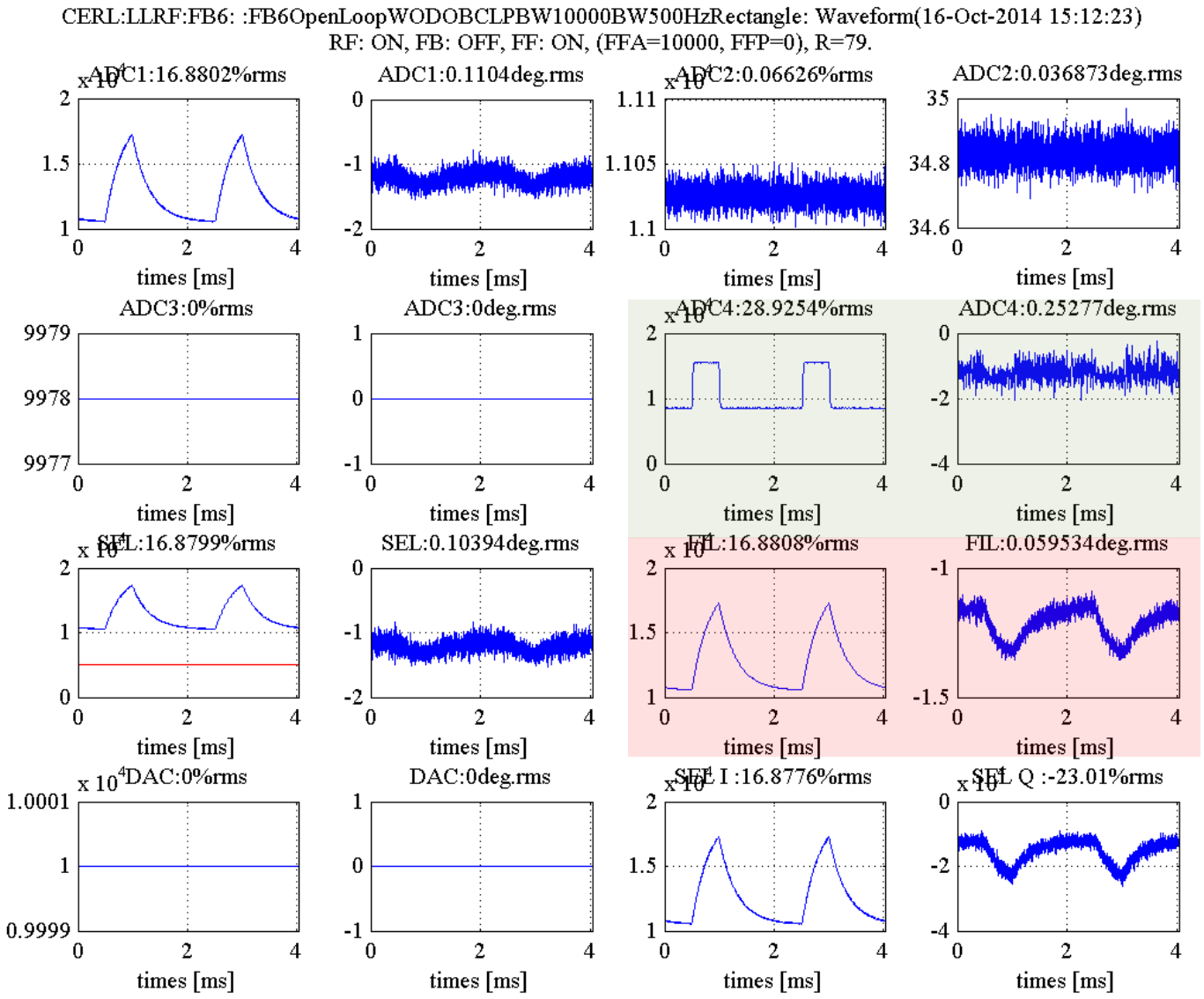
Algorithm（DOBCV4）



FF operation (WO DOBC)

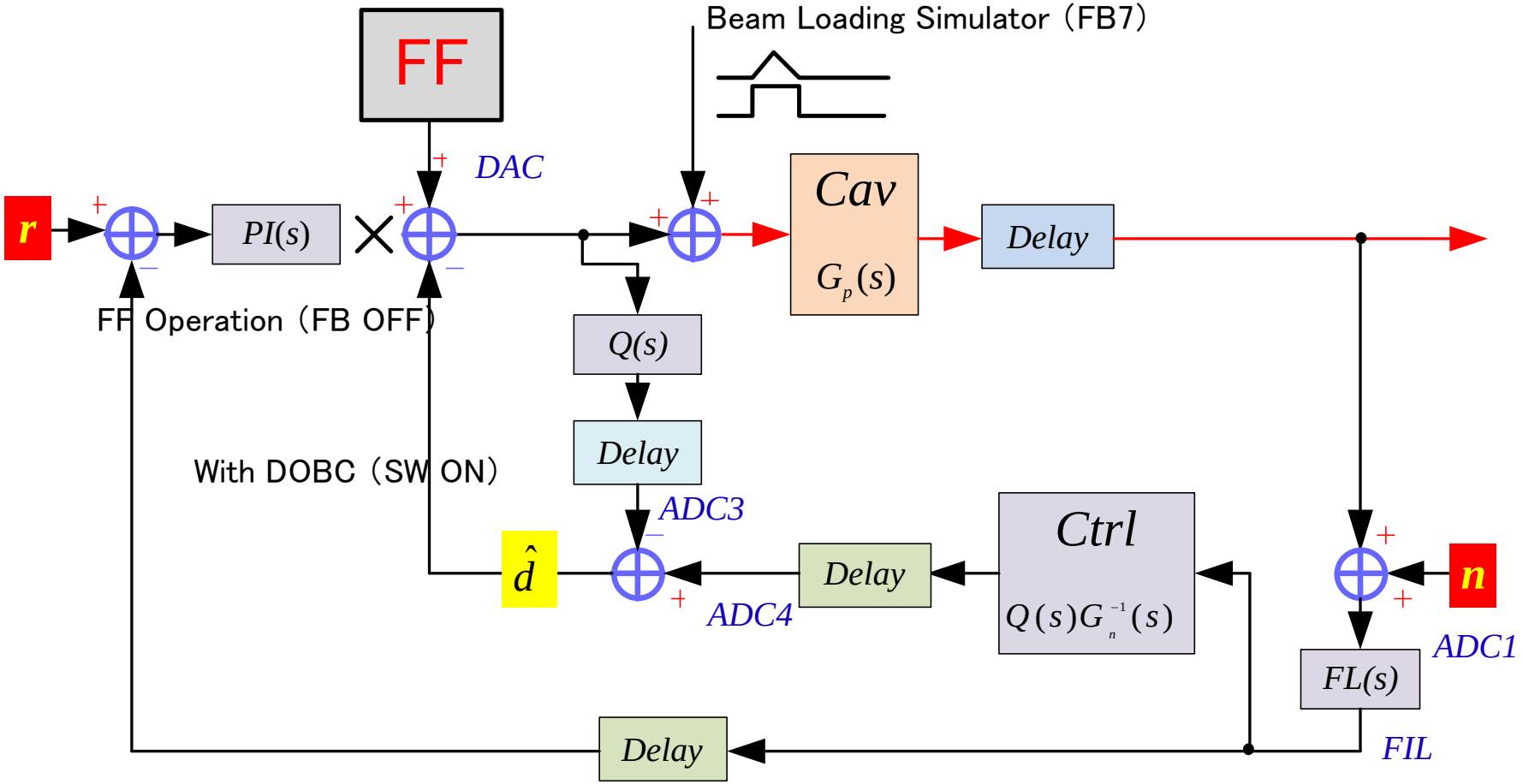


FF operation, WO DOBC

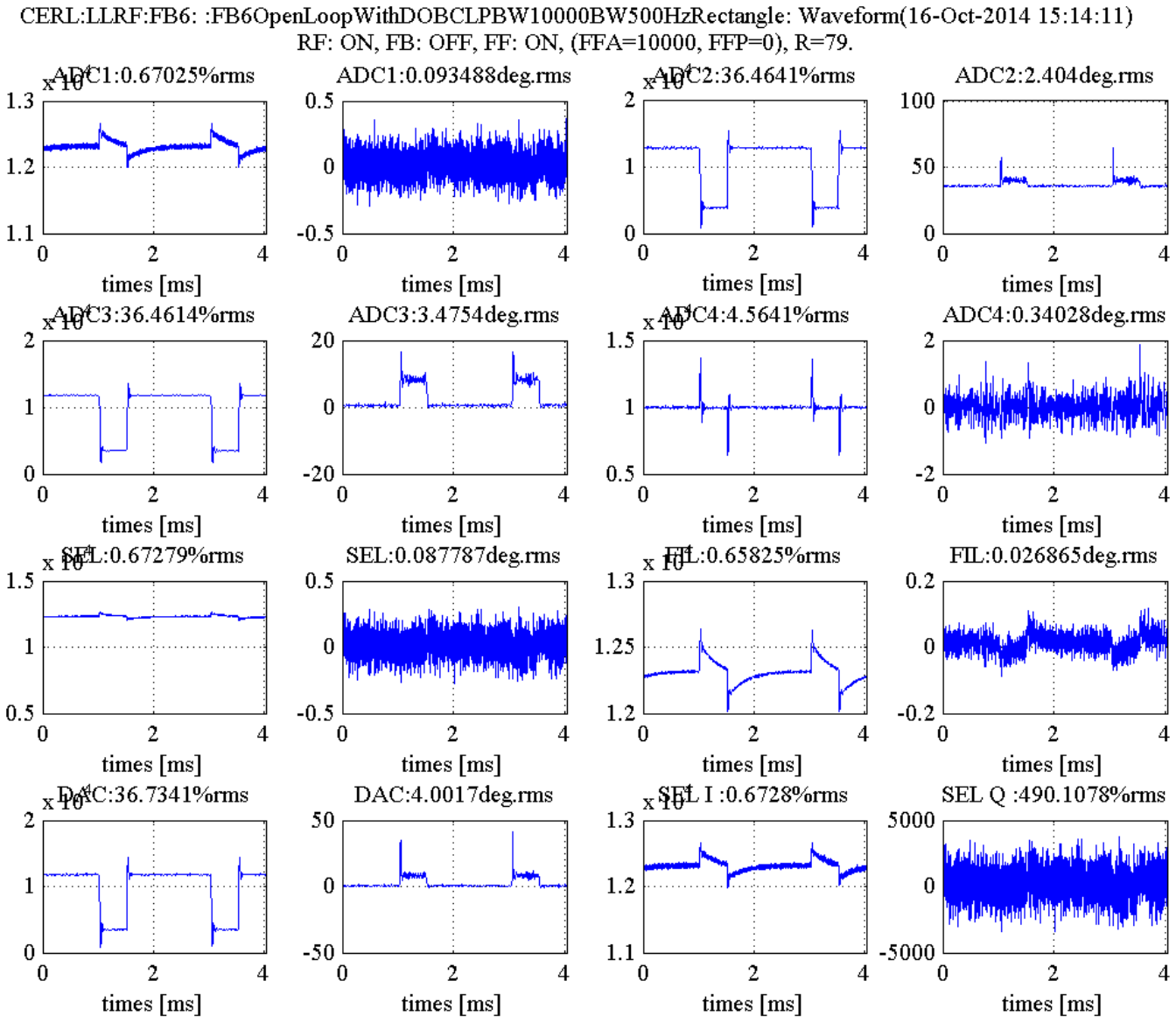


BW=500 Hz (Inj. 1)

FF operation (with DOBC)

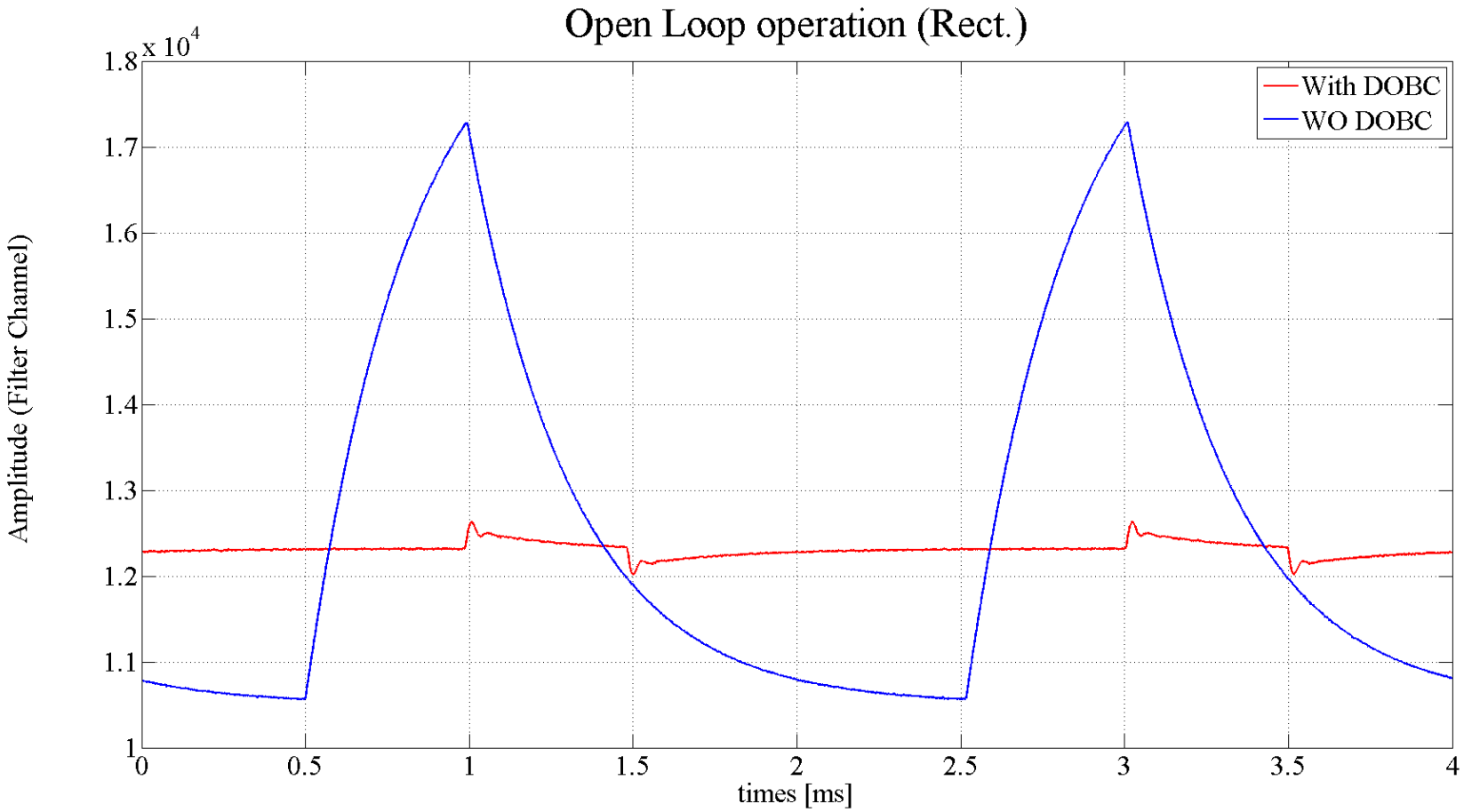


FF operation (with DOBC)

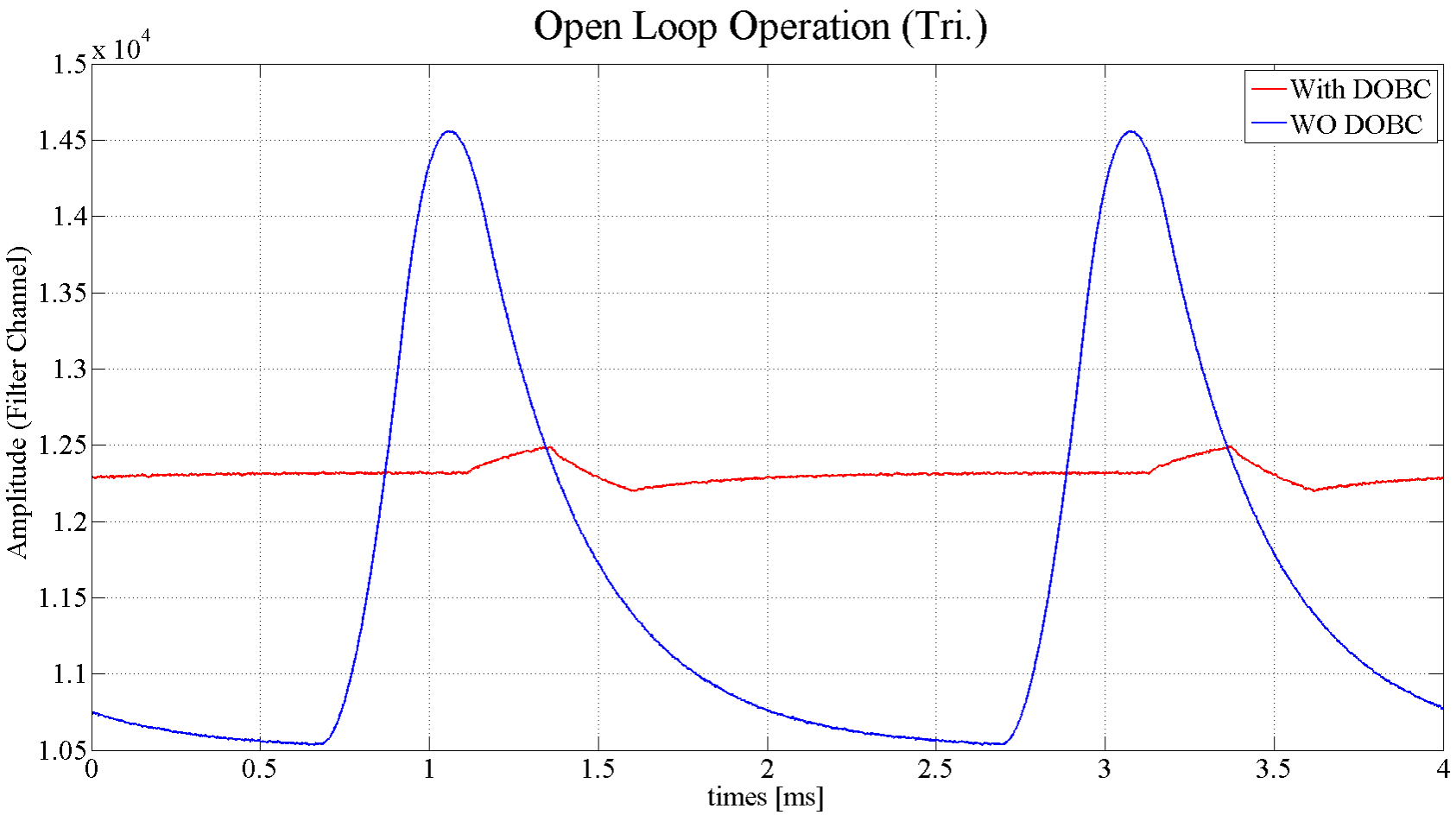


BW=500 Hz (Inj. 1)

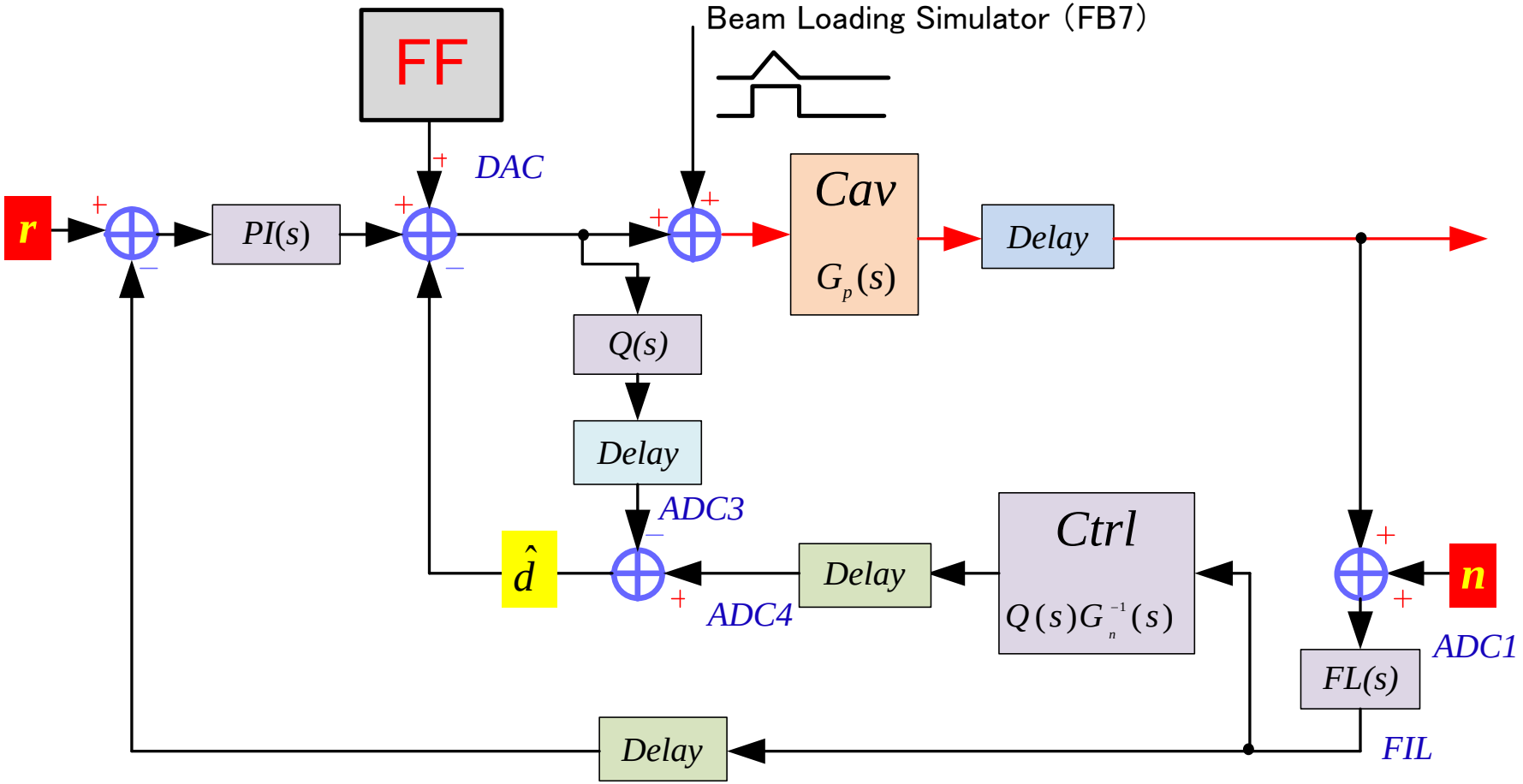
Comparison（FF operation, Rectangle）



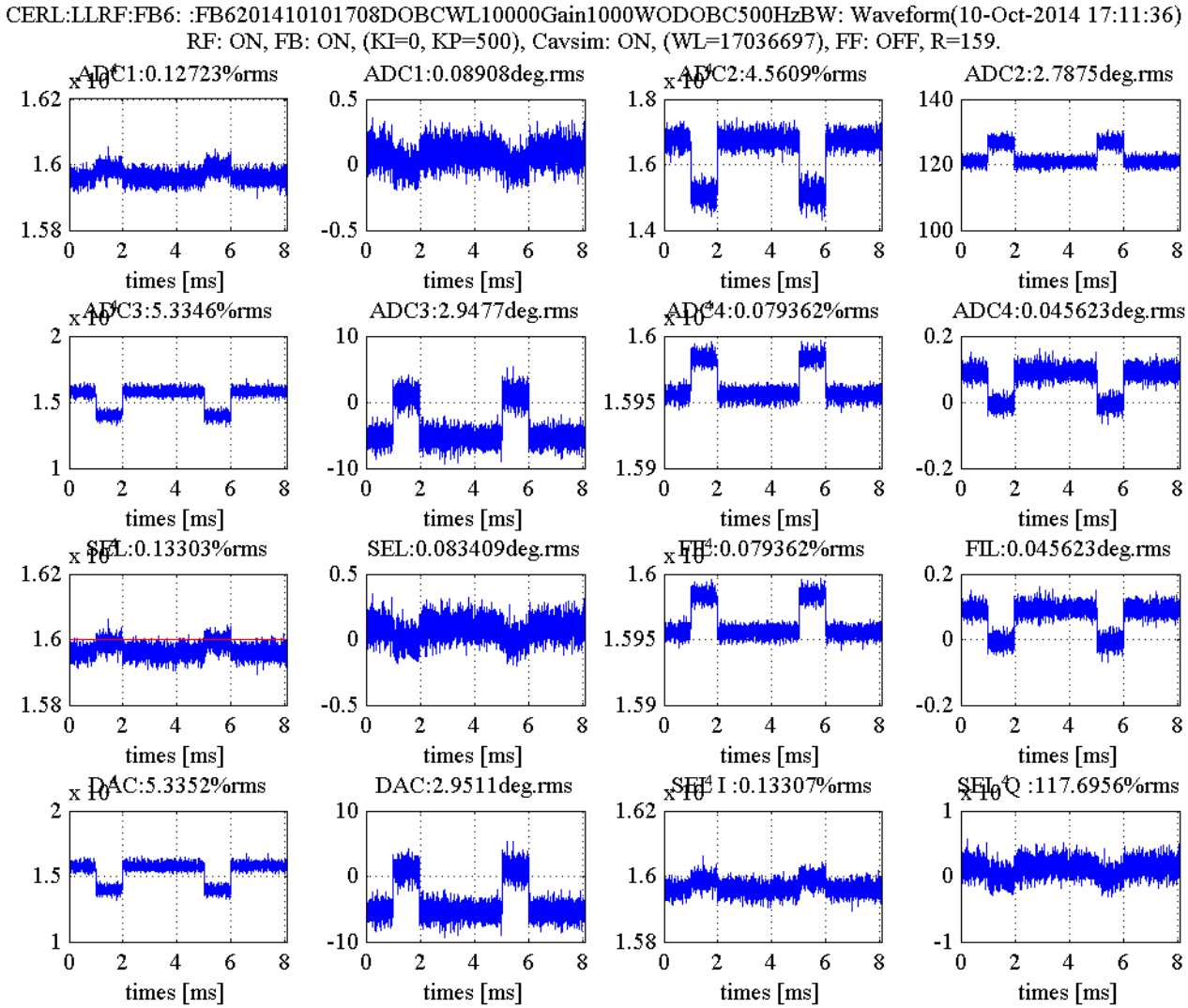
Comparison（FF operation, Triangle）



FB operation

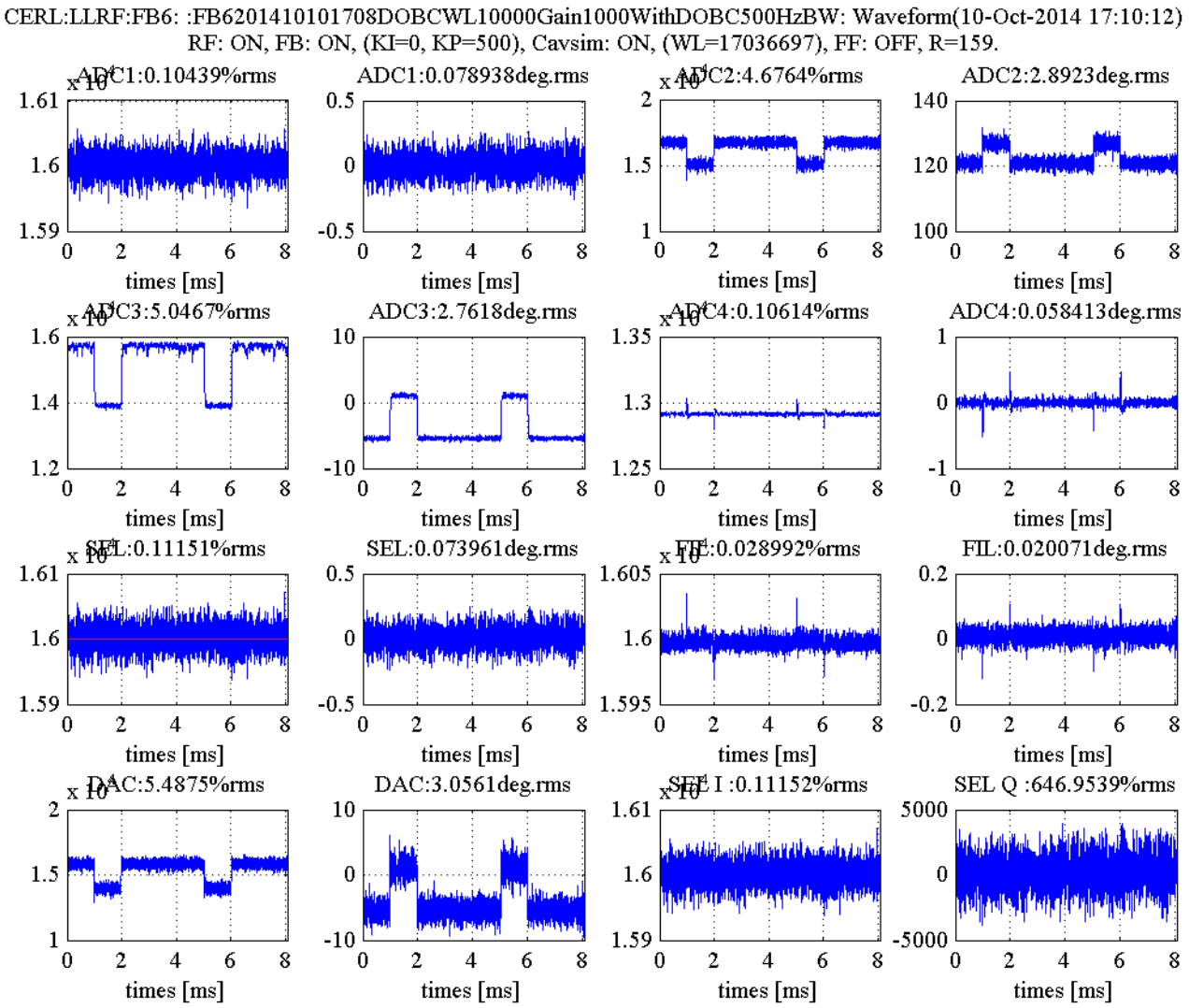


FB operation (WO DOBC)



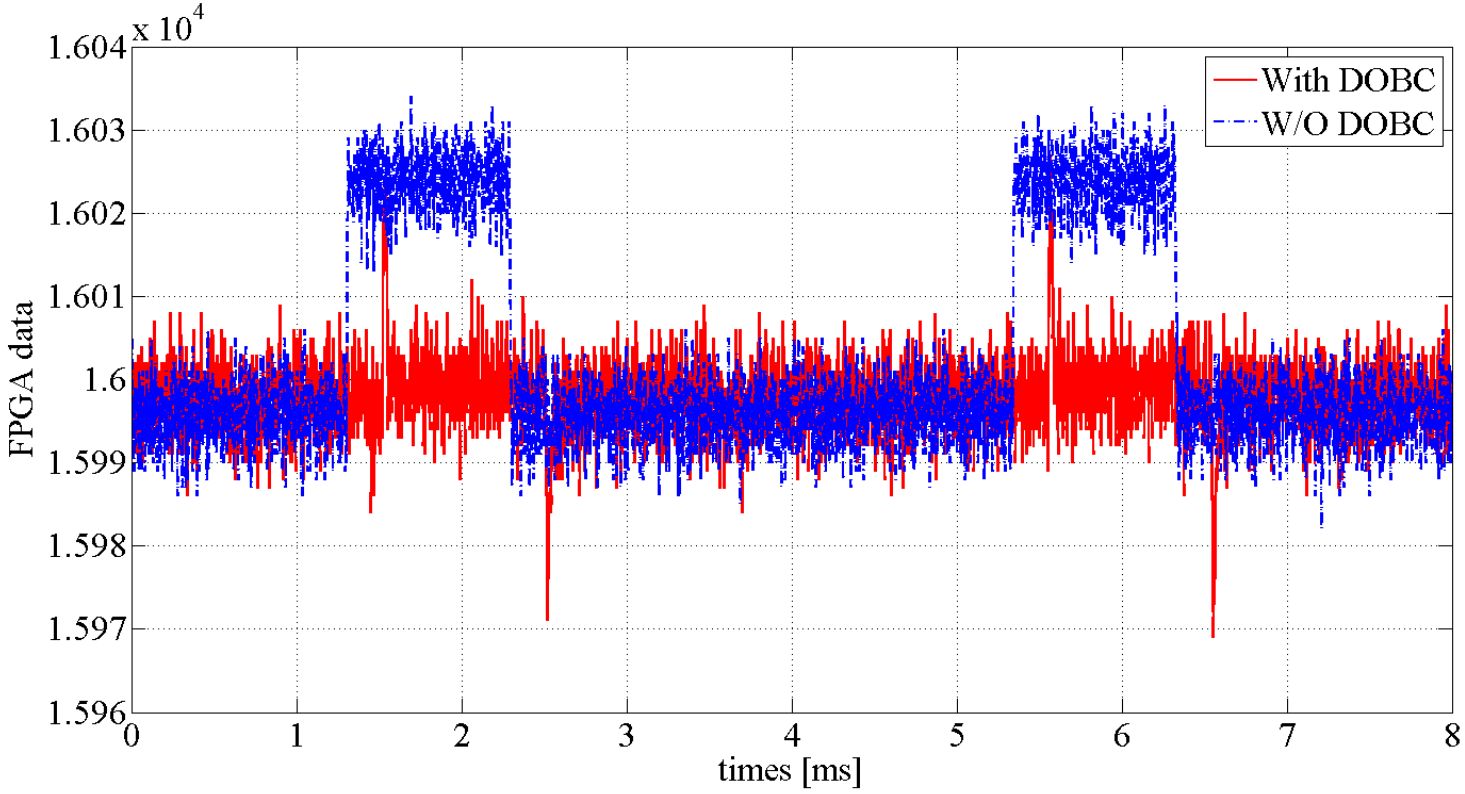
BW=500 Hz (Inj. 1)

FB operation (WO DOBC)



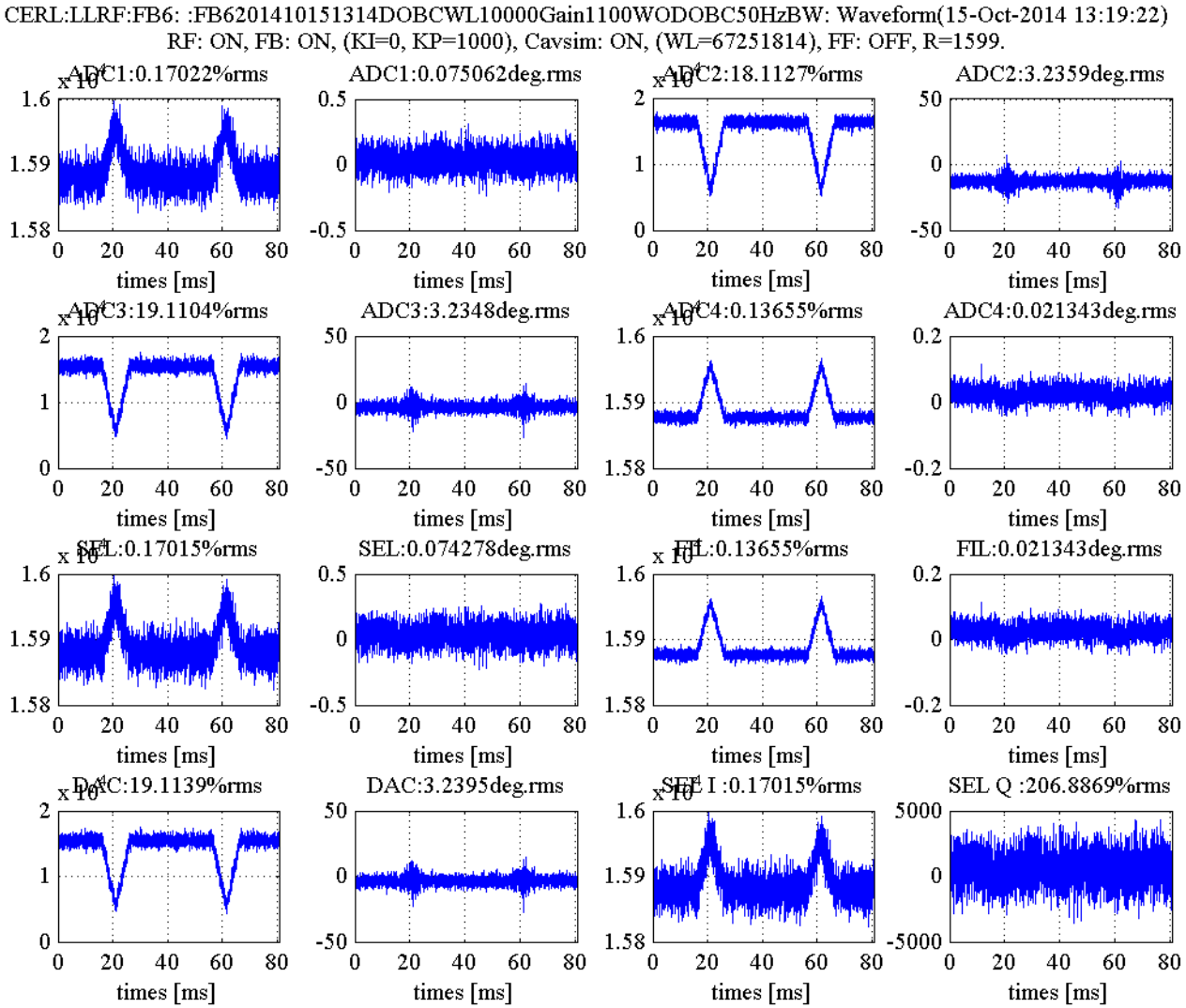
BW=500 Hz (Inj. 1)

FB operation (Rect.)



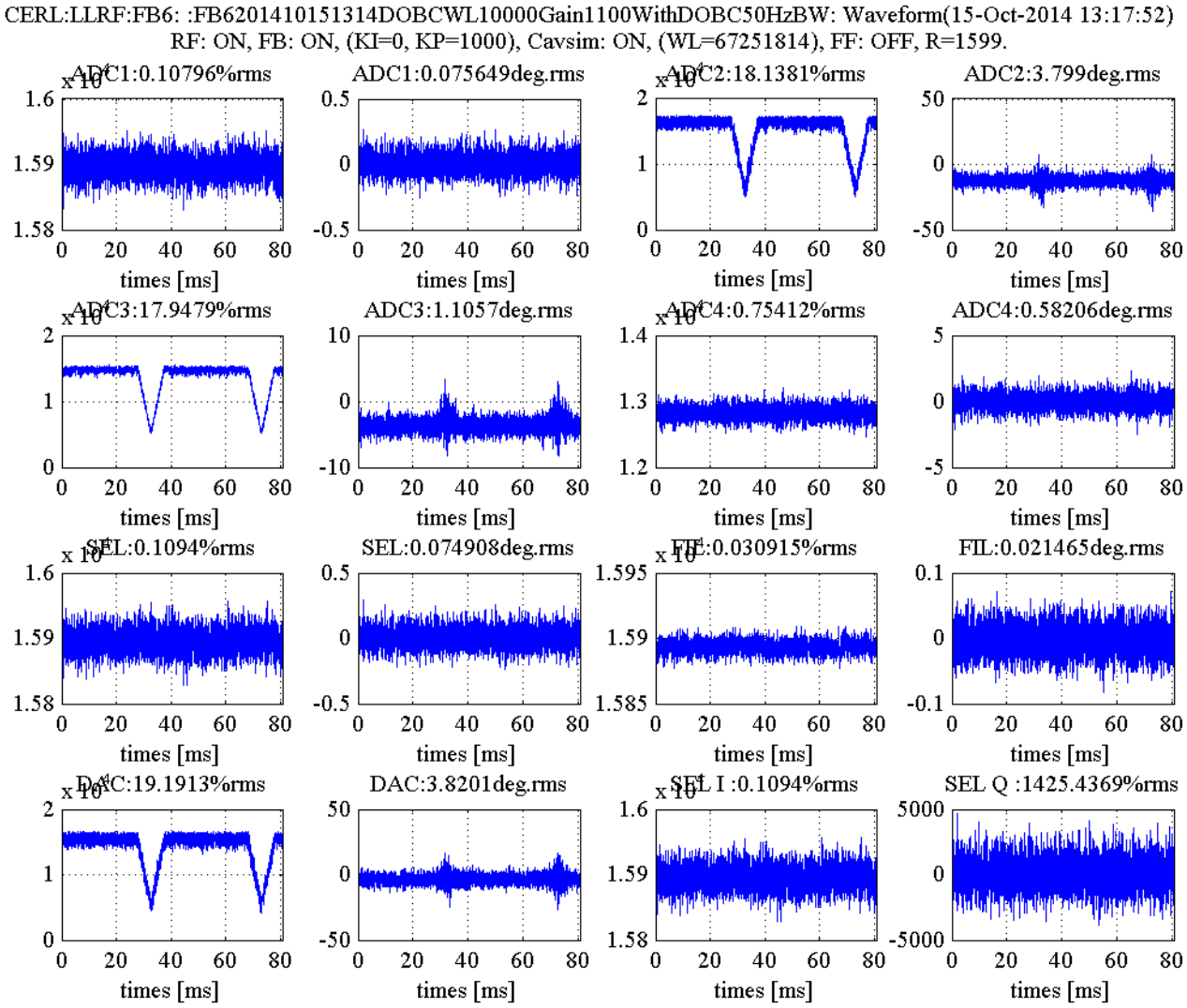
BW=500 Hz (Inj. 1)

FB operation (WO DOBC)



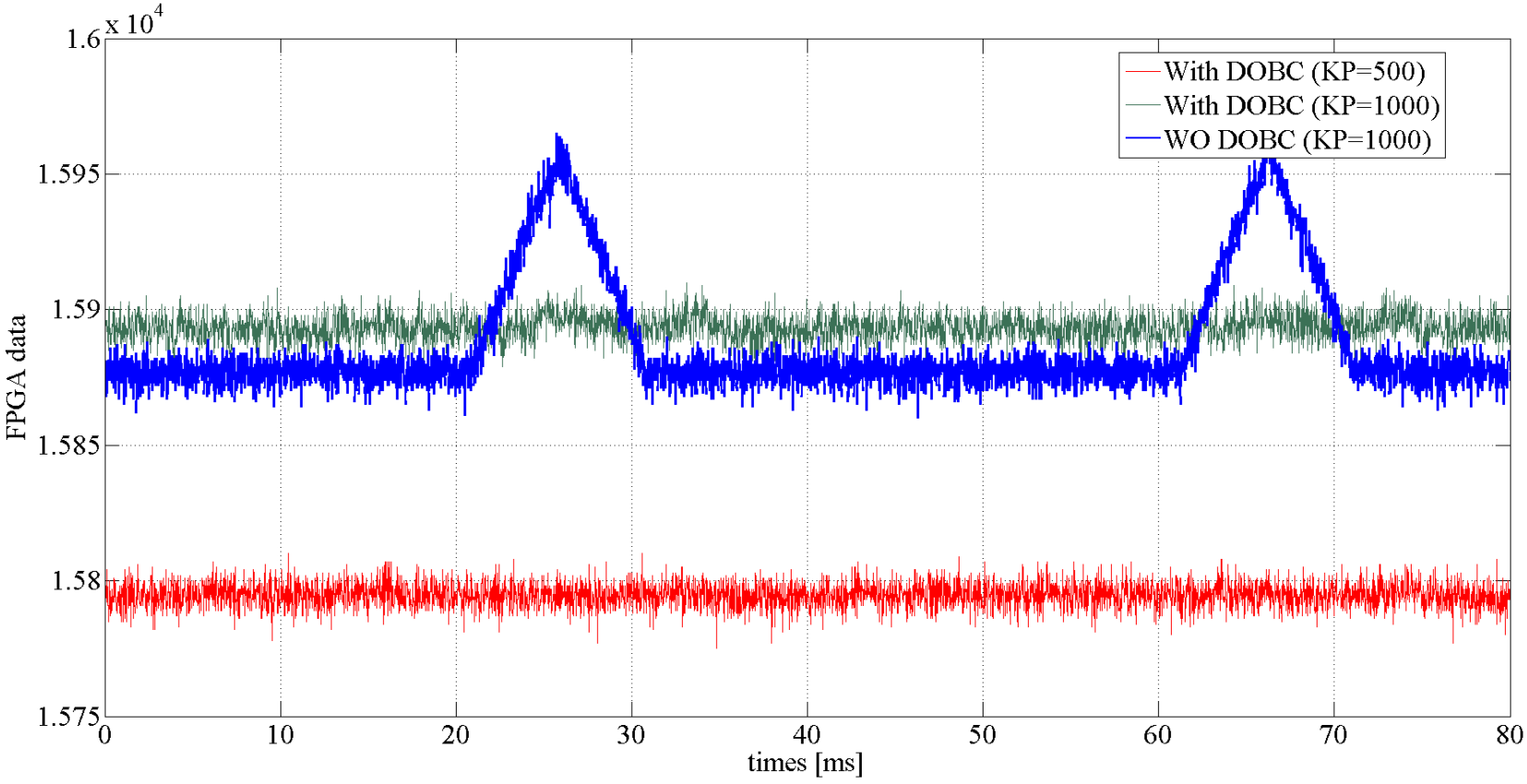
BW=50 Hz (ML 1)

FB operation (With DOBC)



BW=50 Hz (ML 1)

FB operation (Tri.)



BW=50 Hz (ML1)