Scaling of Semiconductor Integrated Circuits and EUV Lithography

(半導体集積回路の微細化とEUVリソグラフィー)

December 13, 2016

EIDEC (Emerging nano process Infrastructure Development Center, Inc.)

Hidemi Ishiuchi

OUTLINE

- Scaling Trend: End of Moore's Law ?
- EUV Lithography: Present Status
- EUV-FEL as light source for EUV Lithography
- Conclusion

"Moore's Law is Dead. Long Live Moore's Law."

WHY NET NEUTRALITY ANALOGIES FAIL
Data is not like water or electricity
P. 10

NUCLEAR POWER'S CROSSROADS
Radical reactors get new attention
P. 12

GORDON MOORE ON MOORE'S LAW:
"I just did a wild extrapolation."
P. 38

TOP 10 TECH CARS
We drive Pagani's $2 million supercar
P. 46

IEEE SPECTRUM

FOR THE TECHNOLOGY INSIDER | 04.15

Moore's Law is dead.

Long live Moore's Law.

IEEE

SPECIAL REPORT

50 Years of MOORE'S LAW

29 The Long Good-bye

30 The Multiple Lives of Moore's Law
Why the rule reigned for half a century—and what will happen next. By Chris Mack

33 Transistors, by the Numbers
A look at six decades of changes in price and production. By Dan Hutcheson

34 Efficiency's Brief Reprieve
Performance gains are declining, but energy efficiency still has some life in it.
By Jonathan Koomey & Samuel Naffziger

37 When Mead Met Moore
Carver Mead talks about his first encounter with the chip visionary. By Rachel Courtland

38 The Law That's Not a Law
A conversation with Gordon E. Moore.

42 Moore's Law Is Dying (and That Could Be Good)
The slowing of transistor miniaturization will benefit many engineers.
By Andrew "bunnie" Huang

Cover and Table of Contents of IEEE Spectrum, vol. 52, issue 4, April 2015

Moore's Law (G. E. Moore, 1965)

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year"

RELATIVE MANUFACTURING COST/COMPONENT

1962

1965

1970

NUMBER OF COMPONENTS PER INTEGRATED CIRCUIT

LOG_2 OF THE NUMBER OF COMPONENTS PER INTEGRATED FUNCTION

YEAR

Ref: Gordon E. Moore, Electronics vol. 38, no. 8, pp. 114-117, 1965

Reprint version: Proc. IEEE vol. 86, no. 1, pp. 82-85, 1998

Moore’s Law after 40 years

(functions per chip, microprocessors)

10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000

1970 1980 1990 2000 2010

2X/2YR
Itanium® 2 Processor
Itanium® Processor
Pentium® III Processor
Pentium® 4 Processor
Pentium® Processor
Pentium® II Processor
386™ Processor
486™ DX Processor
2X/1YR
286
2X/2YR
8086
4004
8080
8008
Past ← → Future

Source: Intel® Corp. ; 2005 ITRS – Seoul Public Conference

Functions /chip: 2x per 2 years

Chip Size Trends – 2005 ITRS Functions/Chip Model IS

2005 ITRS Product Technology Trends
Functions/Chip

(@Volume Production, Affordable Chip Size**)

1.E+03
1.E+02
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06

Product Functions/Chip
(Giga (10^9) - bits, transistors)

Flash Bits/Chip (Gbits) Single-Level-Cell (SLC)
Flash Bits/Chip (Gbits) Multi-Level-Cell (MLC)
MPU GTransistors/Chip - high-performance (hp)
MPU GTransistors/Chip - cost-performanc (cp)
DRAM Bits/Chip (Gbits)

Average Industry "Moores Law"

1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

Year of Production

2005 - 2020 ITRS Range

Past ← → Future

** Affordable Production Chip Size Targets:
DRAM, Flash < 145mm^2
hp MPU < 310mm^2
cp MPU < 140mm^2

Average Industry 1970-2020 "Moore's Law" 2x Functions/chip Per 2 years

MPU ahead or = "Moore's Law" 2x Xstors/chip Per 2 years Thru 2010

** Example Chip Size Targets:
1.1Gt P07h MPU
@ intro in 2004/620mm^2
@ prod in 2007/310mm^2

** Example Chip Size Targets:
0.39Gt P07c MPU
@ intro in 2004/280mm^2
@ prod in 2007/140mm^2

11

Source: ORTC Models; 2005 ITRS – Seoul Public Conference

End of Moore's Law?

Scaling Trend of Logic LSIs

2011 ITRS - Technology Trends

ITRS 2011

1000
100
10
1

Nanometers (1e-9)

1995 2000 2005 2010 2015 2020 2025 2030

Year of Production

- 2009/10/11 ITRS MPU/ASIC Metal 1 (M1) ½ Pitch (nm) [historical trailing at 2-yr cycle; extended to 2013; then 3-yr cycle]
- 2009/10/11 ITRS MPU Printed Gate Length (GLpr) (nm) [3-yr cycle from 2011/35.3nm]
- 2009/10/11 ITRS MPU Physical Gate Length (nm) [begin 3.8-yr cycle from 2009/29.0nm]

16nm

2011 ITRS: 2011-2026

Long-Term '19-'26

Source: ITRS 2011 Edition

End of Moore's Law?

Scaling Trend of Logic LSIs

2011 ITRS - Technology Trends

ITRS 2011 & 2015

1000

100

10

1

Nanometers (1e-9)

2009/10/11 ITRS MPU/ASIC Metal 1 (M1) ½ Pitch (nm) [historical trailing at 2-yr cycle; extended to 2013; then 3-yr cycle]

2009/10/11 ITRS MPU Printed Gate Length (GLpr) (nm) [3-yr cycle from 2011/35.3nm]

2009/10/11 ITRS MPU Physical Gate Length (nm) [begin 3.8-yr cycle from 2009/29.0nm]

"16/14nm"

"11/10nm"

"8/7nm"

"6/5nm"

16nm

ITRS 2015

Metal1 Half Pitch

Physical Gate Length

(High Performance Logic)

1995 2000 2005 2010 2015 2020 2025 2030

Year of Production

2011 ITRS: 2011-2026

Long-Term '19-'26

Source: ITRS 2011 Edition / ITRS 2015 Edition

Cloud and mobile computing drive More Moore

Internet of Things

Big Data and abundant computing power are pushing computing to the **Cloud**

Instant Data generated by sensors and users are pushing computing to the **Edge**

Micro (data) servers and memory

Mobile computing

- Device-interconnect tech should meet microserver and mobile computing needs
- Edge computing requires additional functionality for increased consumer value (e.g. motion processor, neural processor unit, etc)
- 2.5D integration to reduce cost and to scale memory bandwidth / power by pushing memory power < compute power

ITRS 7/13/2015

More Moore FT, ITRS summer meeting, Stanford Univ., Palo Alto, CA, USA, July 11-12, 2015

More Moore computational drivers

Enablers:
Multi-core processors
MPU, GPU, FPGA in single chip
2.5D/3D integration
Wide-IO for memory

Enablers:
Heterogenous integration
Massive parallelism – (many-core)
Cognitive & probabilistic computing
Logic-in memory

Cloud computing
Connectivity of everything
Multi-thread applications
Real-time reconfigurability
Visually rich gaming & browsing
HD streaming
Data accessible everywhere/time

Location awareness & tracking
Emotion/environment recognition
HD-3D conferencing and streaming
Real-time rendering
Personal health-care

PC	Internet	Multimedia & Mobile internet	Virtual reality and location awareness
1990	2000	2010	2020
100M+ units	1B+ units	10B+ units	100B+ units

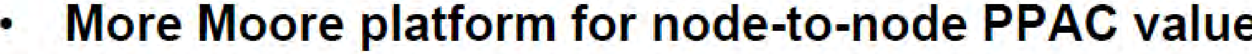
Source: Morgan Stanley Research

Work in Progress – Not for Distribution

Application KPIs and PPAC scaling for More Moore

- **Data/compute servers**
  - KPI = More performance at iso power density
  - Constraints = Thermal, energy budget
- **Edge computing**
  - KPI = More performance & functionality at iso power and cost
  - Constraints = Cost, battery, increased leakage in parallel HW

- **Smart sensors**
  - KPI = Reduced leakage and variability at near-Vt
  - Constraints = System form factor, cost, and security



- **More Moore platform for node-to-node PPAC value**
  - **P**erformance: >25-30% more fmax @ iso power
  - **P**ower: >50% less energy / switching at given performance
  - **A**rea: >50% area reduction
  - **C**ost: <25% wafer cost – ~30% less cost for same function

Work in Progress – Not for Distribution

Performance saturates in conventional scaling

Saturated performance improvement trend, 2013 ITRS

Speed (CV/I)

CV/I (ps)

100
10
1
0.1
0.01

Intel
IEDM
ITRS
2011 Version
FinFET
FDSOI
2013 ver.
Strain
HKMG
HP
III-V (HP, MG)
ITRS
2011

1980 1990 2000 2010 2020 2030

Year

Energy
(CV^2, $W_g=3L_g$)

CV^2 (fJ)

1000
100
10
1
0.1
0.01
0.001

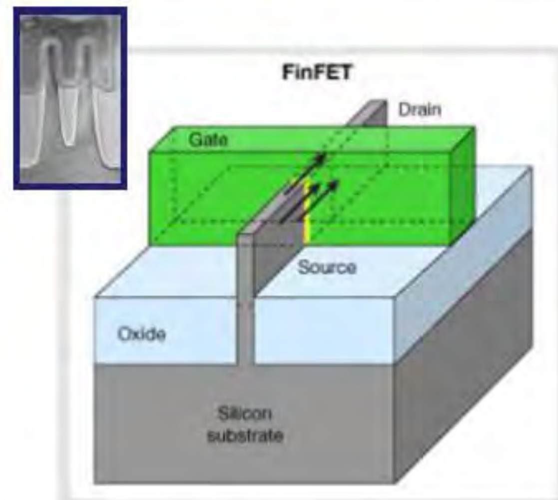
Intel
IEDM
ITRS
2011 Version
FinFET
FDSOI
Strain
2013 ver.
HKMG
HP
III-V (HP, MG)
ITRS
2011

1980 1990 2000 2010 2020 2030

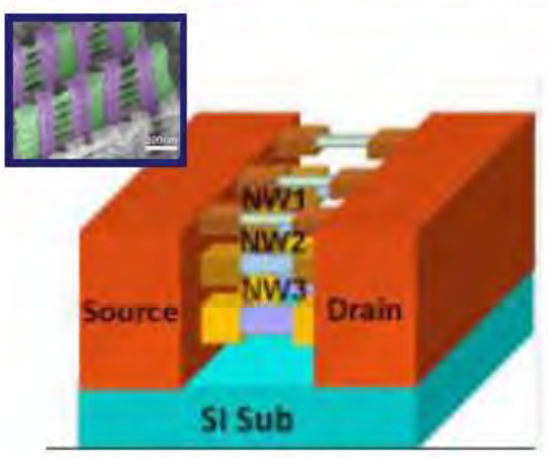
Year

Source ; Prof. Hiramoto, Tokyo Univ.

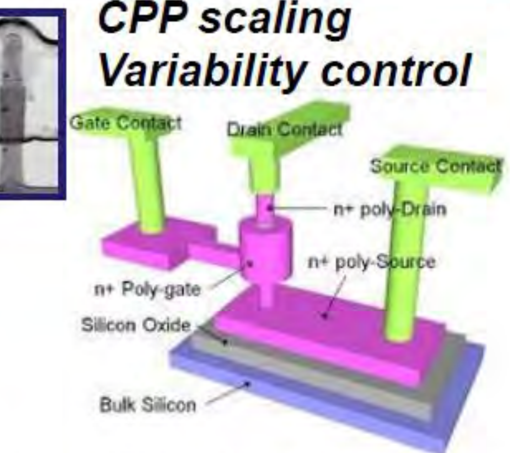
Device architecture evolution to scale CPP



finFET
2011-2019
Lgate/finwidth=3
Weff, SCE

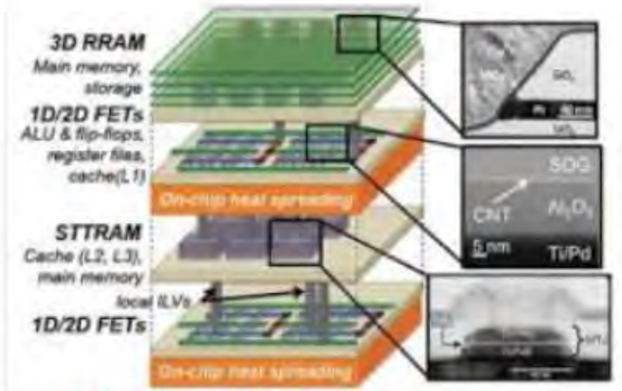


Lateral GAA (gate-all-around)
2018-2024
Lgate/NWD=2
Scale Lgate ~ power reduction



CPP scaling
Variability control

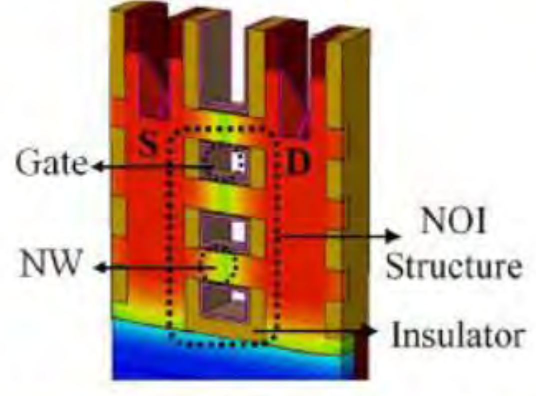
Vertical GAA
2022-2028
Lgate/NWD=2
Variability control, Rext



Monolithic 3D (M3D)
2024-beyond
Lgate/NWD=2
Functional scaling

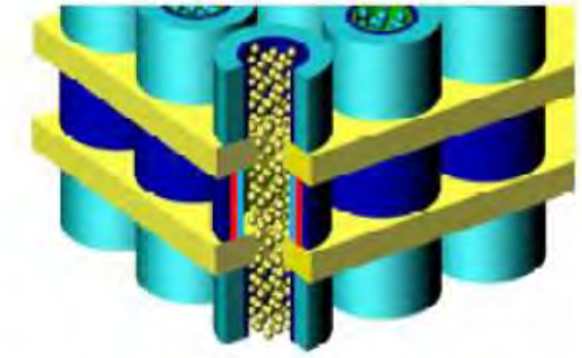
Work in Progress – Not for Distribution

LGAA and VGAA FEP and metrology challenges

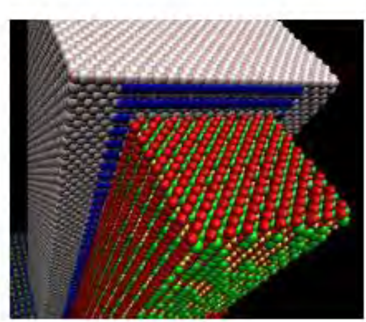


Stacked lateral GAA or NW

S-G. Hur, Samsung



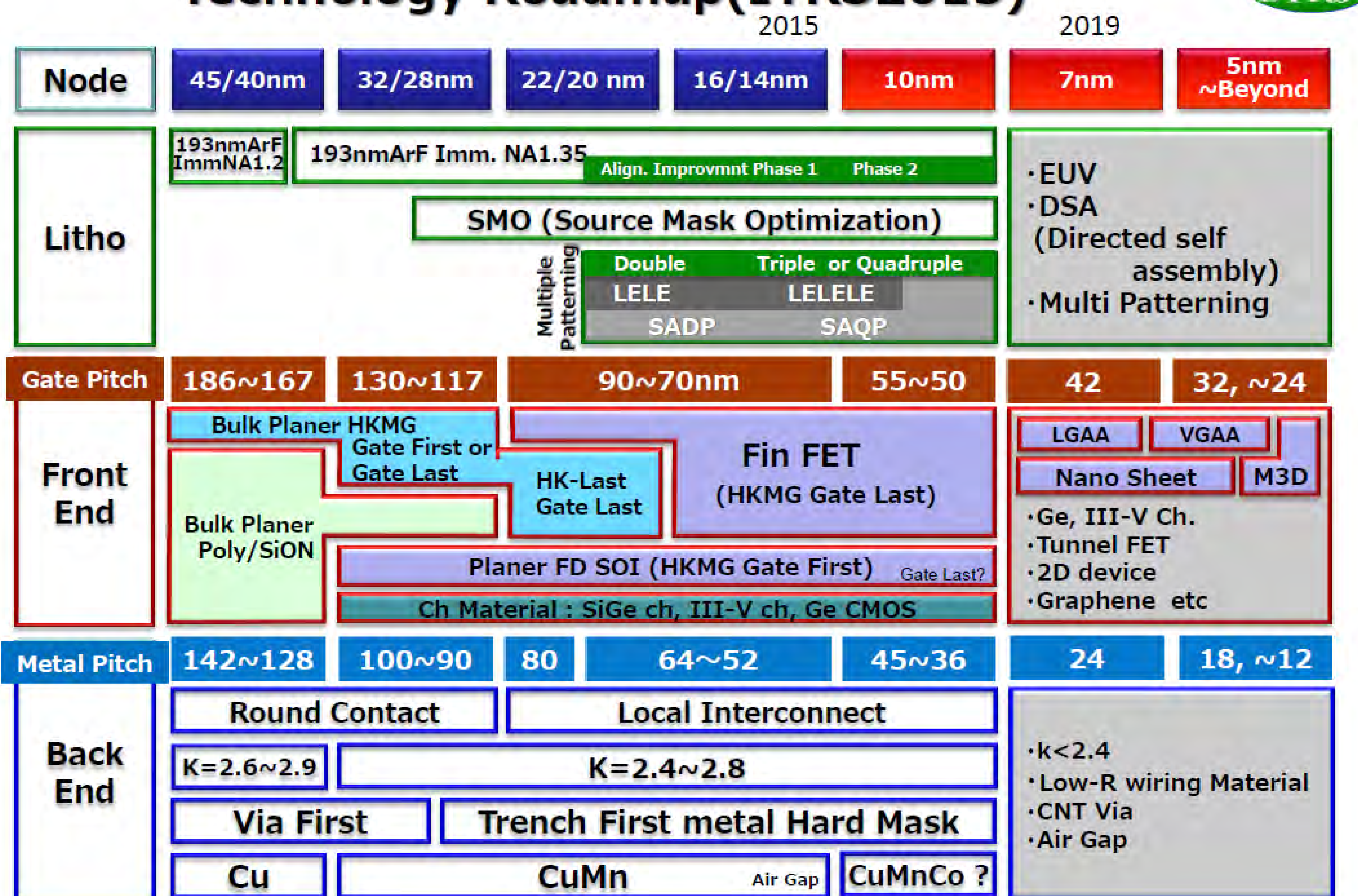
Vertical GAA or NW



Kuhn, Intel, 2012

Stacked NW and GAA structures bring new FEP process challenges
- Conformality
- Integrity
- Reliability
- Controls
- 3D metrology for sub-10nm
- Defectivity
- Yield

Technology Roadmap(ITRS2015)



Work in Progress - Do not publish

STRJ WS: March 4, 2016, WG6

Technology Roadmap Landscape

45/40nm | 32/28nm | 22/20 nm | 16/14nm | 10nm | 7nm | 5nm ~Beyond

Litho

Water Drain
Lens
Water Source
Si Wafer
Wafer Stage
193nm Imm.ArF

Source
Lightening
Co-optimize
Mask
OPC
Source Mask Optimization

Double Patterning(LELE)
Double Patterning(SADP)

Triple Patterning
SAQP

DSA
EUV

Front End

Stress Engineering

HKMG GL
NMOS SiC:P
SiGe P-Ch.
PMOS
SiGe
FDSOI
Fin FET

SiGe Ch
FDSGOI(Pch)
SiCP
Si
BOX
FDSOI(Strain)

Weff boost Fin FET

Ge
SiGe
Si
Ge channel

InGaAs
InP
III-V channel

Horizontal
Gate-All-Around
Vertical

MoS2
SiO2
Si
2D Material

Graphene FET

Back End

K=2.4~2.8
Ultra low-k

14 nm Process
Air Gap

CNT Via

Graphene Wiring

Work in Progress – Not for Distribution

Courtesy: Yuzo Fukuzaki – Sony Corporation

More Moore FT, ITRS summer meeting, Stanford Univ., Palo Alto, CA, USA, July 11-12, 2015

More Complex MOSFET Structure (ITRS 2015)

Node definition: Foundry

2015 2016 2017 | 2020
16nm 10nm 7nm | 5nm 3nm

2y 2y 2y 3y

Node definition: Intel like

2015 2017 2019 2021 2024
~20nm | 14nm 10nm | 7nm 5nm | 3nm~

Bulk Planer
Gate
Drain
Source
Bulk Si

FD-SOI
Gate
Drain
Source
Oxide
Bulk Si

FinFET
Drain
Source
Gate
Oxide
Bulk Si

FinFET limit

EUV introduction

Nanosheet
Drain
Source
Gate
Oxide
Bulk Si

Lateral Gate All Around
Drain
Source
Gate
Oxide
Bulk Si

2D scaling limit

3D functional scaling

Monolithic 3D
Gate
Drain
Epi Si
Source
Gate
Drain
Source
Bulk Si

Monolithic 3D
Gate
Drain
Epi Si
Source
Gate
Drain
Epi Si
Source
Gate
Drain
Source
Bulk Si

Vertical Gate All Around
Drain
Spacer
Gate
Spacer
Source
Bulk Si

Monolithic 3D (CMOS VGAA)
Source
Spacer
Gate
Spacer
Drain
Spacer
Gate
Spacer
Source
Bulk Si

Work in Progress - Do not publish

STRJ WS: March 4, 2016, WG6

EIDEC

Lgate slow-down forcing alt. transport

NCFET

V_G

Ferro-electric, T_{FE}, Metal, High-K Oxide, N+, i-Si, T_{TSOC}, N+, V_D, p- Si, N_{WELL}

V_G, C_{FE}, V_{MOS}, C_{MOS}, C_{ox}, C_{DEP}

Solid Line: w/ FE: V_{DS}=0.3V, V_{DS}=0.4V, V_{DS}=0.5V

Dash Line: w/o FE: V_{DS}=0.3V, V_{DS}=0.4V, V_{DS}=0.5V

~27mV/dec

~165mV/dec

I_{DS} (μA/μm)

V_{GS} (V)

TFET

H -Vs.- V Layout Efficiency

Horizontal

Vertical

V-NWFET Circuit Layout & Design

Tunnel diode rooting

Si shell

c-III/V (N+)

c-SiGe (P+)

Gate overlap

i-Si

L_g

Metal

High-k

P⁺ junction

N⁺ junction

N-well

P-well

TFET Physics

Band Engineering for tunneling

Channel Material – Si Vs. Ge Vs. III-V

Electrostatics

- Quantum simulations

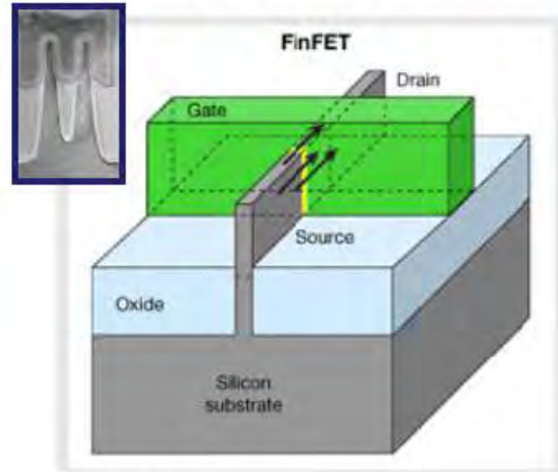
Directed InAs NW on Si(111)

Channel electrostatics & Device Design

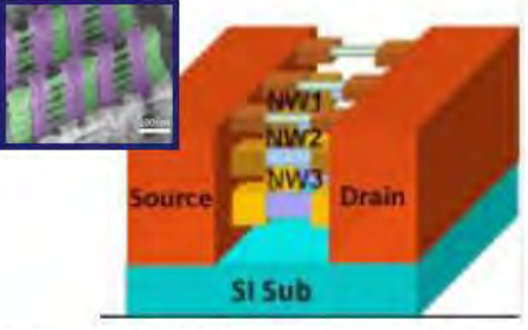
[Source: Yeung (UCB), SISPAD 2012]

[Source: Thean (imec), ITF 2013]

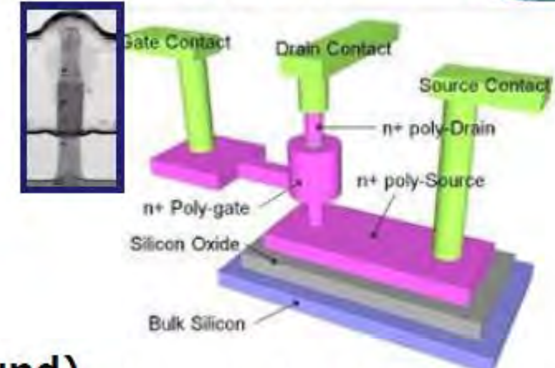
Architecture evolution – key FEP innovations



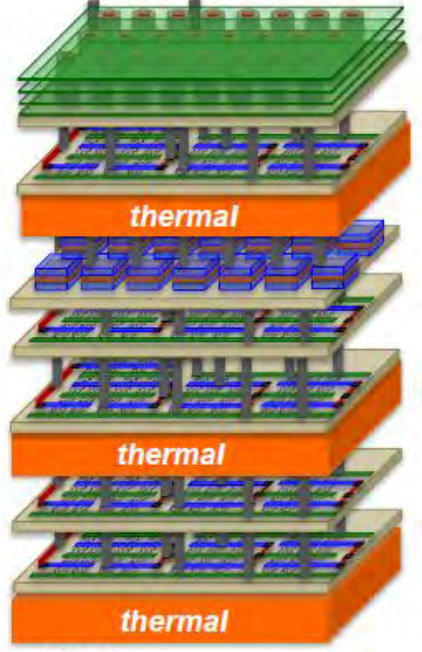
finFET
2011-2019
Lgate/finwidth=3
Weff, SCE



Lateral GAA (gate-all-around)
2018-2024
Lgate/NWD=2
Scale Lgate ~ power reduction



Vertical GAA
2022-2028
Lgate/NWD=2
Variability control, Rext



3D Resistive RAM
Massive storage

1D CNFET, 2D FET
Compute, RAM access

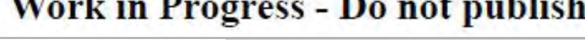
STT MRAM
Quick access

1D CNFET, 2D FET
Compute, RAM access

1D CNFET, 2D FET
Compute, Power, Clock

Monolithic 3D (M3D)
2024-beyond
Lgate/NWD=2
Functional scaling

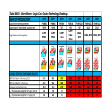
Source: Prof. Mitra, Stanford Univ.



Main scaling focus & performance boosters

Table MM01 - More Moore Device Technology Roadmap								
YEAR OF PRODUCTION	**2015**	**2016**	**2018**	**2020**	**2022**	**2024**	**2026**	**2028**
Logic device technology naming	P70M52	P52M36	P42M24	P32M16	P24M12	P24M12V1	P24M12V2	P24M12V3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"	"1/0.75"
Node production years	3	3	3	3	3	3	3	>3
Device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D	VGAA, M3D
DEVICE ARCHITECTURE & MODULES								
Starting substrate	Si, SOI	Si, SOI	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW	Si,SOI, SRB, QW
N-channel	Si	sSi	sSi, Ge	sSi, sGe, IIIV	sSi, sGe, IIIV	sSi, sGe, IIIV	sSi, sGe, IIIV	sSi, sGe, IIIV
P-channel	Si	Si,SiGe	Si,SiGe	Si,SiGe	Ge	Ge	Ge	Ge
Channel formation	Etch	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI	Etch, EPI
Contact material	Silicide	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH	Low-SBH
Contact integration	EPI	EPI	EPI WAC	EPI WAC	EPI WAC	EPI WAC	EPI WAC	EPI WAC
DEVICE PERFORMANCE BOOSTERS								
Main performance booster	SCE finHeight Vt	SCE finHeight Vt	Parasitics finHeight	Parasitics finHeight	Low Vdd 3D	Low Vdd 3D	Low Vdd 3D	Low Vdd 3D
Scaling focus	Perf	Power	Power	Power	Function	Function	Function	Function
Channel strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
S/D strain	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Transport scheme	DD	Quasi Ballistic	Quasi Ballistic	Ballistic	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS	Ballistic TFET, JFET, NCMOS, Spin	Ballistic TFET, JFET, NCMOS, Spin

- Increasing Functions/$ is the main focus
- Added new node naming nomenclature (e.g. P70M52) since pitch scaling is not directly representing node itself
- 2014-2018 (N14, N10) focus on SCE, Weff scaling, cell height reduction
- 2018-2022 (N7 and N5) focus on parasitics, Weff scaling, active utilization in standard cell
- 2022-2030 (N3 and beyond) focus on ultra low-Vdd and 3D integration



Scaling of MOSFET

Table MM01 - More Moore - Logic Core Device Technology Roadmap							
YEAR OF PRODUCTION	**2015**	**2017**	**2019**	**2021**	**2024**	**2027**	**2030**
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
	FinFET FDSOI	FinFET FDSOI	Lateral Nanowire FinFET	Vertical Nanowire Lateral Nanowire	Vertical Nanowire Monolithic 3D	Vertical Nanowire Monolithic 3D	Vertical Nanowire Monolithic 3D
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12

finFET: fin Field Effect Transistor

FDSOI: Fully Depleted Silicon On Wafer

LGAA: Lateral Gate-All-Around

VGAA: Vertical Gate-All-Around

M3D: Monolithic 3 Dimensional

Source: ITRS 2015 Edition, “More Moore” Chapter, Table MM01

Ground rules

YEAR OF PRODUCTION	2015	2016	2018	2020	2022	2024	2026	2028
Logic device technology naming	P70M52	P52M36	P42M24	P32M16	P24M12	P24M12V1	P24M12V2	P24M12V3
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Node production years	3	3	3	3	3	3	3	>3
Device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D	VGAA, M3D
LOGIC DEVICE GROUND RULES								
Contacted gate pitch (nm)	70	52	42	32	24	24	24	24
L_g : Physical Gate Length for HP Logic (nm)	24	18	14	10	10	10	10	10
L_g : Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12	12
Spacer width (nm)	12	8	6	5	5	5	5	5
Contact CD (nm) - finFET, LGAA	22	18	16	12	-	-	-	-
Metal pitch (nm)	56	36	24	18	12	12	12	12
finFET - lateral pitch (nm)	42	27	24	18				
LGAA - lateral pitch (nm)			24	18				
LGAA - vertical pitch (nm)			18	18				
VGAA - lateral pitch (nm)				18	12	12	12	12
Fin width (nm)	8	6	6	6				
Lateral GAA - nanowire diameter (nm)			7	5				
Vertical GAA - nanowire diameter (nm)				5	5	5	5	5
Fin height (nm)	40	35	35	35				
Number of active lateral GAA devices vertically stacked			3	2				
Footprint drive efficiency - finFET	2.10	2.81	3.17	4.22				
Footprint drive efficiency - lateral GAA			2.75	1.75				
Footprint drive efficiency - vertical GAA				0.87	1.31	1.31	1.31	1.31
PATTERNING								

- Gate pitch slowing to extend life of lateral devices
- Area scaling compensated by metal scaling
- Contact CD=12nm is the limit to keep Rext within limits
- Vertical GAA loses 3D device knob to scale Weff – loss compensated by monolithic 3D
- Lgate and CPP scaling slow-down stops Capa down-scaling – ultra low-Vdd is needed

3D Cell Arrays of NAND Flash Memories

ISSCC2014, Three-Dimensional 128Gb MLC Vertica NAND Flash-Memory with 24-WL Stacked Layers and 50MB/s High-Speed Programming, Ki-Tae Par et al.

Charge Trap Cell (Samsung)

Control Gates (0V)

Source Select Gate (De-biased relative to Source)

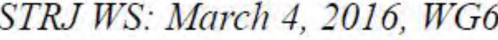
N+ Source (Erase Voltage)

Floating Gate Cell (intel / Micron)

(b)

IEDM2015, A Floating Gate Based 3D NAND Technology with CMOS under Array (Invited), Krishna Parat et al

Work in Progress - Do not publish



Rayleigh's Formula

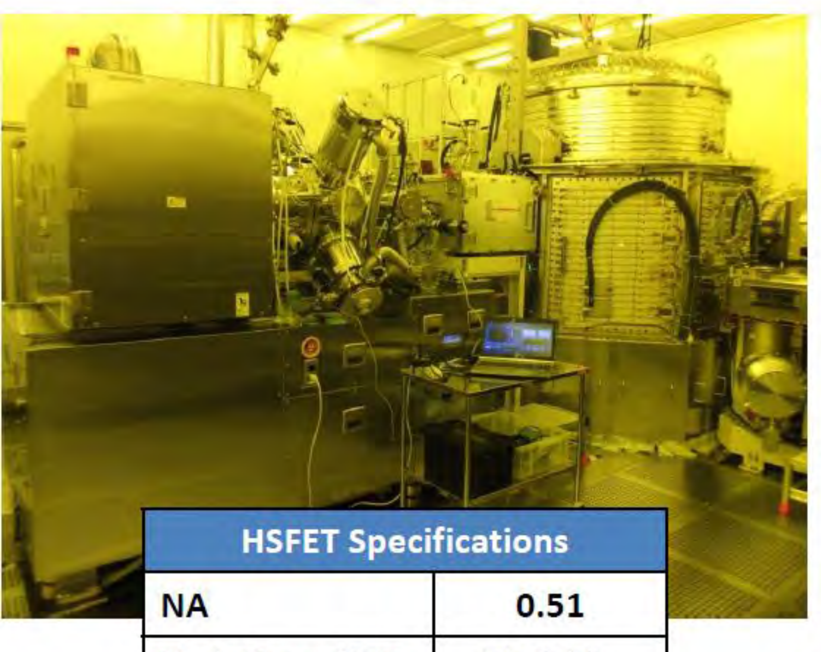
$$R = k_1 \frac{\lambda}{\mathrm{NA}}$$

R: Resolution (nm)
k_1: Constant
λ: Wave Length (nm)
NA: Numerical Aperture

R **(nm)**	k_1	λ **(nm)**	NA
64	0.31	193 (ArF)	0.93
37	0.26	193 (ArF)	1.35
12	0.30	13.5 (EUV)	0.33
7.9	0.30	13.5 (EUV)	0.51
7.3	0.30	13.5 (EUV)	0.55

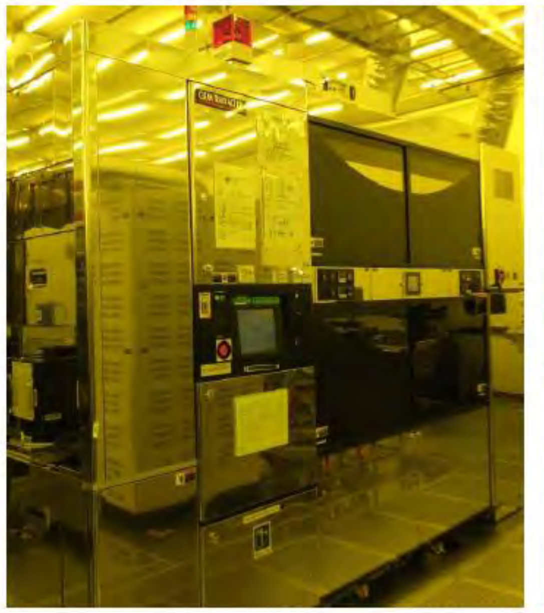
EUV Lithography Tools in AIST SCR

EUV Small Field Exposure Tool HSFET



HSFET Specifications	
NA	0.51
Variation of NA	Variable
Illumination	σ_{max}=1.0 (6 apertures)
Field Size	0.03x0.2mm

Clean Track ACT12



CD-SEM CG4000

AIST Open Research Platform
https://unit.aist.go.jp/tia-co/orp/index_en.html

AIST : National Institute of Advanced Industrial Science and Technology
SCR : Super Clean Room

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Variable NA – NA0.33 vs. NA0.51

HSFET Image Contrast vs. L&S hp size

13nm

Contrast

L&S hp size [nm]

Dipole45 NA0.51

Dipole45 NA0.33 (HSFET)

0th Order Light

1st Order Light

15nm LS

13nm LS

11nm LS

Center Obscuration

NA Aperture

NA0.33

NA0.51

	15nm LS	14nm LS	13nm LS	12nm LS	11nm LS
NA0.33					
NA0.51					

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

HSFET Image Contrast (Simulation)

HSFET Image Contrast vs. L&S hp size

13nm

NA=0.51

Contrast

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

0 5 10 15 20 25 30

L&S hp size [nm]

—Quadrupole
—Dipole for 22nm Pitch
—Dipole for 16nm Pitch

Illumination shape (schematics)

denotes center obscuration area in PO

Quadrupole

Dipole for 22nm Pitch

Dipole for 16nm Pitch

- ✓ **Quadrupole illum. will show better resolution performance for over 14nm hp patterning.**
- ✓ **Dipole illum. will show better performance for under 13nm hp patterning.**

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Imaging Performance - Quad. Illumination

24nm L/S

22nm L/S

20nm L/S

18nm L/S

16nm L/S

14nm L/S

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Imaging Performance - Dipole for 11nm L/S

12nm L/S

11nm L/S

10nm L/S

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Imaging Performance - Leaf Dipole for 8nm L/S

11nm L/S

10nm L/S

9.5nm L/S

9.0nm L/S

Source: S. Magoshi, et al,, "Recent status of the High-NA Small Field Exposure Tool (HSFET) at EIDEC," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

193i multi-patterning cost explosion

Patterning Cost

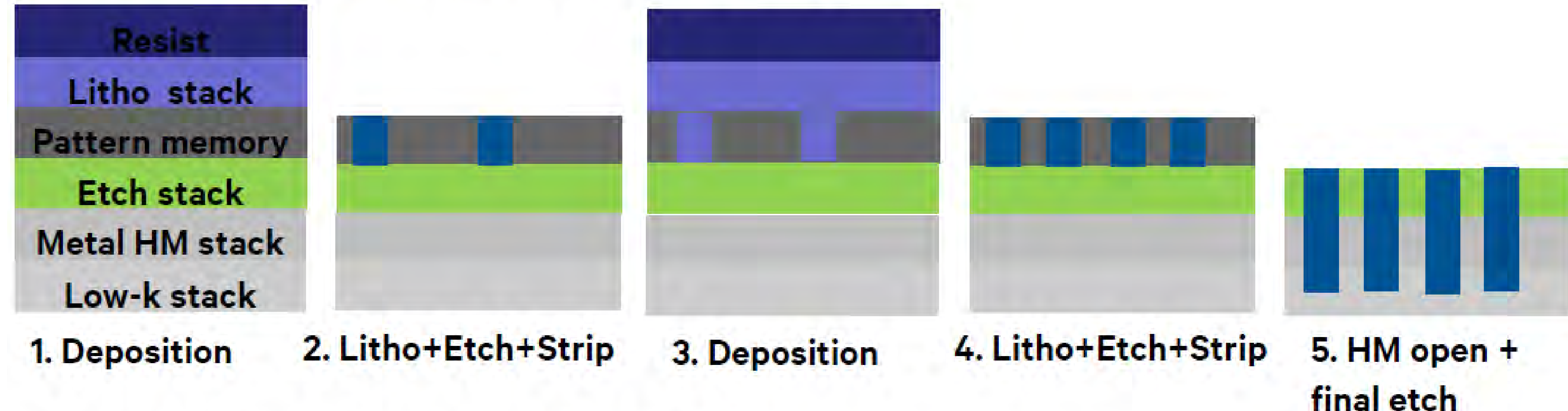
Option	Metal LE / Via LE	Metal LELE / Via LE	Metal LELELE / Via LELE	Metal SADP +2cuts / Via LE	Metal SAQP +2cuts / Via LELELE
Cost	$				$$$$$

Need for 193i litho stack simplification through innovative materials

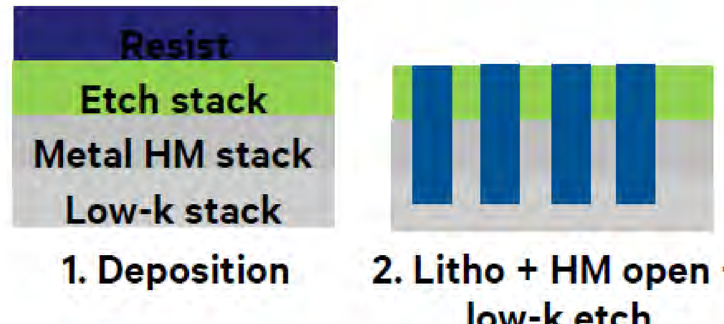
Work in Progress – Not for Distribution

EUV - simplifying stack and saving steps

193i LELE metal patterning



EUV SE metal patterning



Pros
- Simplified stack
- Avoiding CDU and OVL seen in MPT
- Less # of depo, litho, etch steps

Cons
- Need improvements in resists for productivity and better LER

Work in Progress – Not for Distribution

“10nm Technology” of Samsung

Design	10 nm	14 nm
Gate pitch	64 nm	78 nm
CA pitch	64 nm	78 nm
Active Contact Width	18 nm	20 nm
M1, Mx (Metal Interconnect) pitch	48 nm	64 nm

- Metal (M1, Mx) half pitch: 24 nm
- Lithography Tool: ArF immersion (ArF-i)

Ref: H.-J. Cho, et al, 2016 Symposium on VLSI Technology, Digest of Technical Papers, pp.14-15, 2016.

“7 nm Technologies” in IEDM 2016

- IBM, GLOBALFOUNDRIES, and Samsung:
  - Poly Si (contacted): 44nm / 48 nm pitch （ArF-i）
  - Metal interconnect: 36nm pitch （EUV)
  - EUV lithography for Metal Interconnect
- TSMC:
  - SRAM cell size: 0.027 um^2
  - ArF immersion (ArF-i) lithography
    (R&D with EUV Lithography, too)

Ref: IEDM Technical Digest, 2016

IEDM 2016, #2.6, IBM/GF/Samsung

7nm MOL & BEOL Design Space Enabled by EUV
EUV
LE^n
2D
Layout
High-NA EUV
SADP
DSA
1D
SATP
SAQP
7nm FIN with SAQP
7nm Gate with SADP
50
40
30
20
Minimum pitch (nm)

Fig. 7. 7nm patterning approaches.

Ref: IEDM Technical Digest, 2016

IEDM 2016, #2.6, IBM/GF/Samsung

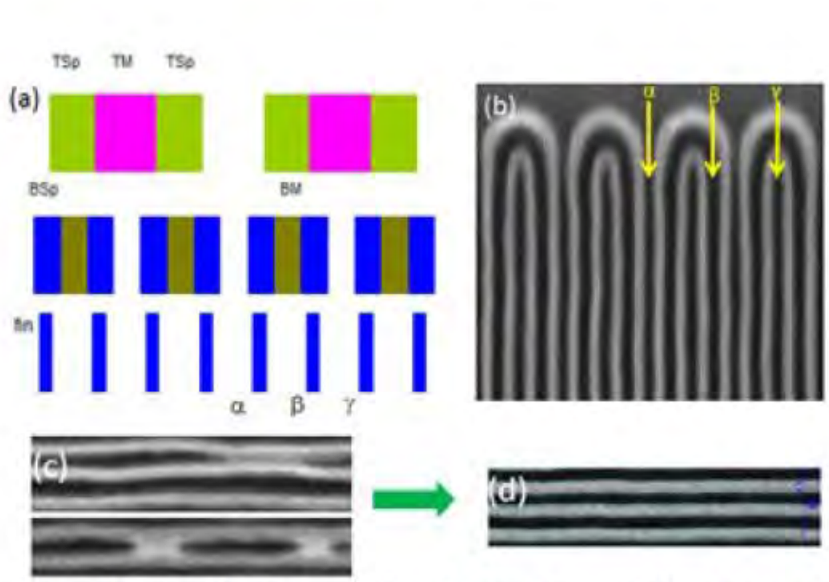


Fig. 8. (a) Schematic flow for self-aligned quadruple FIN patterning (SAQP); (b) Topdown SEM of the FINs formed with SAQP process. (c) un-optimized vs (d) Optimized SAQP process.

Fig. 12. (a)(b) Improved common process window in DOF and printing resolution achieved with EUV, compared to optical litho. (c)(d) Topdown SEMs of typical MOL EUV patterning with 45°, 90° cross-couple, respectively (24nm trench width).

Ref: IEDM Technical Digest, 2016

2016 EUVL Symposium: Highlights

Source

- ✓ 70% average availability achieved. (champion: 90% per 4wks)
- ✓ 1500 wpd demonstrated but consistency is the next challenge.

Resist

- ✓ Sensitivity and LER/LCDU are far from targets.
- ✓ Stochastic variation needs to be addressed for current and future materials.

Source: "Closing Address," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 26, 2016

2016 EUVL Symposium: Highlights

Mask

- ✓ Very positive year (ABI optic upgraded, AIMS tool shipped).
- ✓ Blank suppliers making progress (0 defect blanks possible).
- ✓ Infrastructure gap for pattern mask inspection.

Pellicle (keeping mask clean)

- ✓ Good progress but very far to go for HVM readiness.
- ✓ Need industry focus to bring all the required components together.

Source: "Closing Address," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 26, 2016

2016 EUV Focus Areas

Key Focus Areas	Rank*	StdDev
Reliable source operation with > 85% availability	2.00	1.09
Resist resolution, sensitivity & LER met simultaneously	2.14	1.01
Keeping mask defect free (by pellicle and affiliated infrastructure)	2.36	0.88
Mask yield & defect inspection/review infrastructure	3.50	0.78

**) Average of 22 steering committee members' votes*
1 being the most critical

Source: "Closing Address," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 26, 2016

EUV Focus Areas

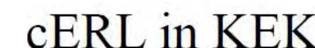
2013 / 22hp	2014 / 16hp	2015 / 16hp	2016 / 16hp
1. Long-term reliable source operation with a. 125 W at IF in 2014 b. 250 W in 2015	1. Reliable source operation with > 75% availability – 125 W at IF in 1H / 2015 (at customer) – 250 W at IF in 1H / 2016 (HVM entry at customer)	1. Reliable source operation with > 85% availability – Expectation of 1500 average wafers per day in 2016	1. Reliable source operation with > 85% availability – 1500 wafers per day with consistency in 2017
2. Mask yield & defect inspection/review infrastructure	2. Resist resolution, sensitivity & LER met simultaneously – Progress insufficient to meet 2015 introduction target	2. Resist resolution, sensitivity & LER met simultaneously – Increased focus needed on manufacturing performance (defectivity, pattern collapse,...)	2. Resist resolution, sensitivity & LER met simultaneously – Sensitivity and LER/LCDU are far from targets. – Stochastic variation needs to be addressed for current and future materials
4. Keeping mask defect free – Availability of pellicle mtg HVM req't – Minimize defect adders during use	3. Mask yield & defect inspection/review infrastructure – Enable high yield defect free mask blank supply chain	3. Mask yield & defect inspection/review infrastructure – Sustainability of mask tool supply chain remains critical	3. Keeping mask defect free – Good progress but very far to go for HVM readiness – Need industry focus to bring all the required components together
4. Resist resolution, sensitivity & LER met simultaneously	3. Keeping mask defect free – Availability of pellicle mtg HVM req't : need integrated industry strategy for solution – Minimize defect adders during use	4. Keeping mask defect free (by EUV pellicle) - Pellicle demonstration in the field (on 3300) required in 2016	4. Mask yield & defect inspection/review infrastructure – Infrastructure gap for pattern mask inspection remains

Source: "Closing Address," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 26, 2016

EUV-FEL (Free Electron Laser)

Achieved values in cERL and Design values at the EUV-FEL

Items	Achieved values in cERL	Design Values at the EUV-FEL
Energy for injector (MeV)	2.9-6	10.5
Energy of Accelerator(MeV)	20	800
Charge /bunch (pC)	0.7-5	60
Repetition rate (MHz)	162.5-1300	162.5
Average Current (mA)	1.0	9.75
Emitance for electron beam (mm mrad)	0.3-1	0.6
Gradient of the accelerated energy (MV/m)	8.6	12.5
Wavelength of EUV-FEL (nm)	/	13.5
Average power of EUV-FEL (kW)	/	Higher than 10 kW



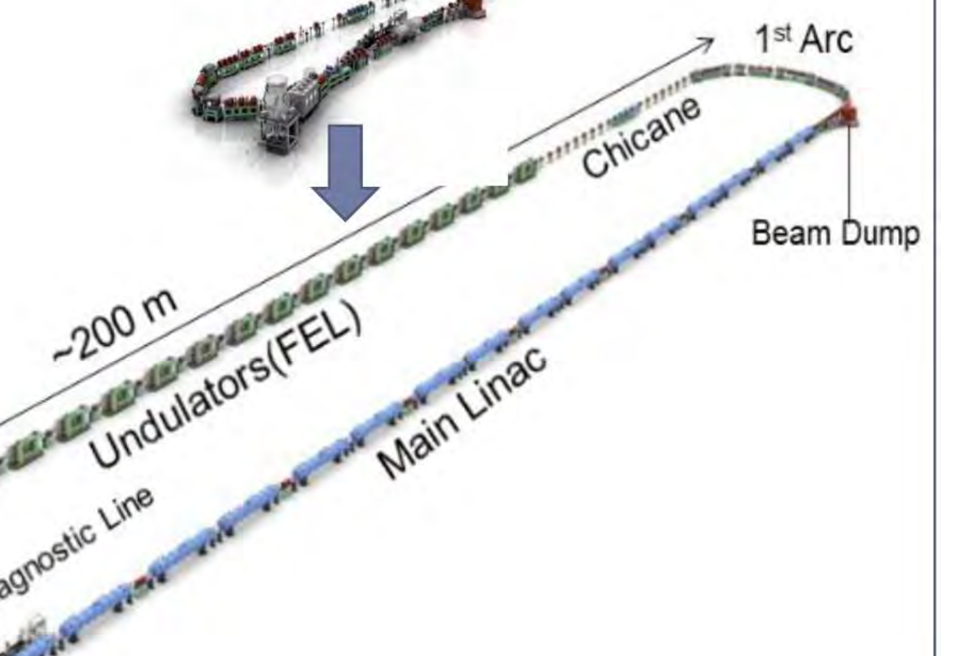


Fig. 2 Prototype design of the EUV-FEL

Source: H. Kawata, "Strategy to realize the EUV-FEL high power light source," 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Potential Problems in EUV-FEL

- R&D expense to develop EUV-FEL
  - Who pays the cost? International collaboration necessary.
  - When and where available?
- Cost of ownership
  - to be less expensive than existing EUV source
- Foot print
- Stable operation
  - two beam lines are necessary for back up
- Generation of radioactive materials due to high energy electron irradiation
- High peak power
  - potential damage in mirrors and reticles
  - Resist
- Too coherent EUV light

Tradeoff: Resolution vs Sensitivity

Background

Metal resist
(Cornell univ.)
Poor
Resolution
High
Metal resist
(EIDEC)
CAR NTI (Negative-tone)
CAR PTD (Positive-tone)
Trade-off line
Target !
Metal resist
(Inpria)
High
Low
Sensitivity

2016 International Symposium on Extreme Ultraviolet Lithography, Oct 24th- 26th , 2016

FUJIFILM

Low sensitivity is acceptable if higher EUV source power is available.

Ref: 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan

Summary

- Scaling limit is 10nm for MOSFET gate length; 6nm for metal interconnect, according to ITRS 2015.
- Performance and degree of integration will be getting better by using new device structures, new materials, 3D device structure, 3D assembly & packaging, etc. even if we reach the scaling limit
- EUV lithography will be used in mass production tool for 7nm or 5nm logic products and beyond.
- EUV-FEL is a possible solution as an EUV source with higher average power than 1 kW. Its cost of ownership, peak power, coherence of the EUV-FEL source might be the potential problems to be solved

References

- ITRS (International Technology Roadmap for Semiconductors)
  - http://www.itrs2.net/
  - ITRS latest version, and archives
  - White Paper, Presentation Materials, etc.

- JEITA / STRJ (Semiconductor Technology Roadmap committee of Japan)
  - http://semicon.jeita.or.jp/STRJ/
  - ITRS 2013 Edition (Japanese version) and older
  - Presentation material of STRJ Workshop, etc.

- SEMATECH and ISMI Proceedings Archives: Lithography
  - http://www.sematech.org/meetings/archives/litho/index.htm

- IEUVI (International EUV Initiative)
  - http://ieuvi.org/index.html
  - http://ieuvi.org/TWG/IEUVI_TWGs01.htm