Present Status and Future Prospects of EUV Lithography

(EUV リソグラフィーの現状と将来展望)

December 11, 2011

Evolving nano process Infrastructure Development Center, Inc.
（EIDEC)

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Outline

- Scaling Trend: End of Moore's Law ?
- Present Status of EUV Lithography
- Challenges in EUV Lithography
- Mass Production with EUV Lithography
- Summary

IRDS Lithography Roadmap

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
DRAM							
DRAM minimum ½ pitch (nm)	18	17.5	17.0	14.0	11.0	8.4	7.7
Flash							
2D Flash ½ pitch (nm) (un-contacted poly)	15	15	15	15	15	15	15
3D NAND minimum array 1/2 pitch (nm)	80	80	80	<80	<80	<80	<80
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
MPU/ASIC Minimum Metal ½ pitch (nm)	18.0	14.0	12.0	10.5	7.0	7.0	7.0
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Lateral Gate All Around (LGAA) 1/2 pitch			12.0	10.5	9.0		
Vertical Gate All Around (VGAA) half pitch (nm)						7.0	7.0
Vertical GAA Diameter (nm)						6.0	6.0
Chip size (mm^2)							
Maximum exposure field height (mm)	26	26	26	26	26	26	26
Maximum exposure field length, i.e. scanning direction (mm)	33	33	33	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm^2)	858	858	858	429	429	429	429

No scaling needed after2027 or 2030 ?

DRAM still shrinking

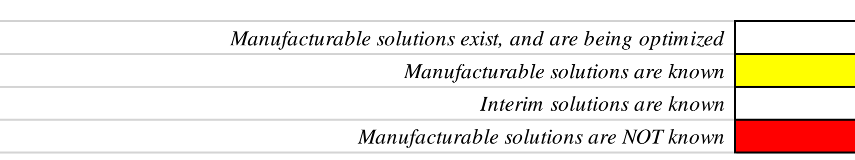
Flash is no longer a driver for high resolution patterning

Logic is driving patterning

Small holes for VGAA

High-NA(0.55) EUV exposure tool with a reduced field size: 858 mm^2 → 429mm^2

Source: "IRDS 2017 Edition, Lithography," Table LITH-1 (2018)



3D Cell Arrays of NAND Flash Memories

ISSCC2014, Three-Dimensional 128Gb MLC Vertical NAND Flash-Memory with 24-WL Stacked Layers and 50MB/s High-Speed Programming, Ki-Tae Park et al.

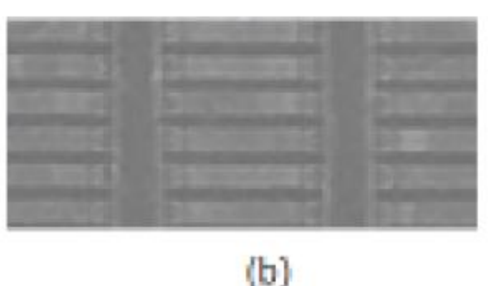
Charge Trap Cell (Samsung)

Control Gates (0V)

Source Select Gate (De-biased relative to Source)

N+ Source (Erase Voltage)

Floating Gate Cell (intel / Micron)



(b)

IEDM2015, A Floating Gate Based 3D NAND Technology with CMOS under Array (Invited), Krishna Parat et al

Contact hole pattern in DRAM

"EUV single exposure process can be applied below D1z node or beyond."

hp22, 47mJ/cm2 | hp24, 36mJ/cm2 | hp24, 49mJ/cm2

CD : 26.6 ± 2.6nm | CD : 25.3 ± 2.5nm | CD : 30.3 ± 2.2nm

15 images / dose, 120 holes / image | 15 images /dose, 90 holes / image | 15 images /dose, 90 holes / image

Fig. 5 SEM top view images and CD measurement results at the conditions indicated by arrows in Fig. 4. Outer 2 lanes of holes are excluded in CD measurement in order to avoid proximity effect of the boundary.

Source: Mijuing Lim et al., "EUV contact-hole local CD uniformity optimization for DRAM storage node application," SPIE Advanced Lithography, 2018; Proc. SPIE 10583, Extreme Ultraviolet (EUV) Lithography IX, 105830X (1 May 2018); doi: 10.1117/12.2299322

More Complex MOSFET Structure (ITRS 2015)

Node definition: Foundry

2015 2016 2017 | 2020
16nm 10nm 7nm | 5nm 3nm

Node definition: Intel like

2y 2y 2y 3y
2015 2017 2019 2021 2024
~20nm | 14nm 10nm | 7nm 5nm | 3nm~

Bulk Planer
Gate
Drain
Source
Bulk Si

FD-SOI
Gate
Drain
Source
Oxide
Bulk Si

Stress技術
SiGe Ch.(P)

FinFET
Drain
Source
Gate
Oxide
Bulk Si

FinFET limit

EUV introduction

Nanosheet
Drain
Source
Gate
Oxide
Bulk Si

実効W長
ブースト

Lateral Gate All Around
Drain
Source
Gate
Oxide
Bulk Si

2D scaling limit

3D functional scaling

Monolithic 3D
Gate
Drain
Epi Si
Source
Gate
Drain
Source
Bulk Si

Monolithic 3D
Gate
Drain
Epi Si
Source
Gate
Drain
Epi Si
Source
Gate
Drain
Source
Bulk Si

レイヤ数ブースト

Vertical Gate All Around
Drain
Spacer
Gate
Spacer
Source
Bulk Si

Monolithic 3D
(CMOS VGAA)
Source
Spacer
Gate
Spacer
Drain
Spacer
Gate
Spacer
Source
Bulk Si

実効W長 ブースト

Work in Progress - Do not publish

STRJ WS: March 4, 2016, WG6

Multiple Patterning with ArF immersion tools

Double Exposure

Mask 1

Resist
Device layer
Substrate

Expose trenches

Mask 2

Expose trenches

Develop and etch

Double Patterning

Mask 1

Resist
Hardmask
Device layer
Substrate

Print trenches and etch hardmask

Mask 2

Coat and expose second resist

Etch hardmask and device layer

Spacer double patterning

Mask 1

Top Hard Mask
Buffer Oxide
Bottom Hard Mask
Substrate

Top hardmask etch
Spacer formation

Oxide deposition
CMP

Spacer removal
Oxide removal
Bottom hardmask etch

Figure LITH2 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

Source: ITRS 2013 Edition, Lithography, Figure LITH2

EUV vs ArF immersion: process complexity

EUV reduces multi-pattern process complexity

Process steps per layer

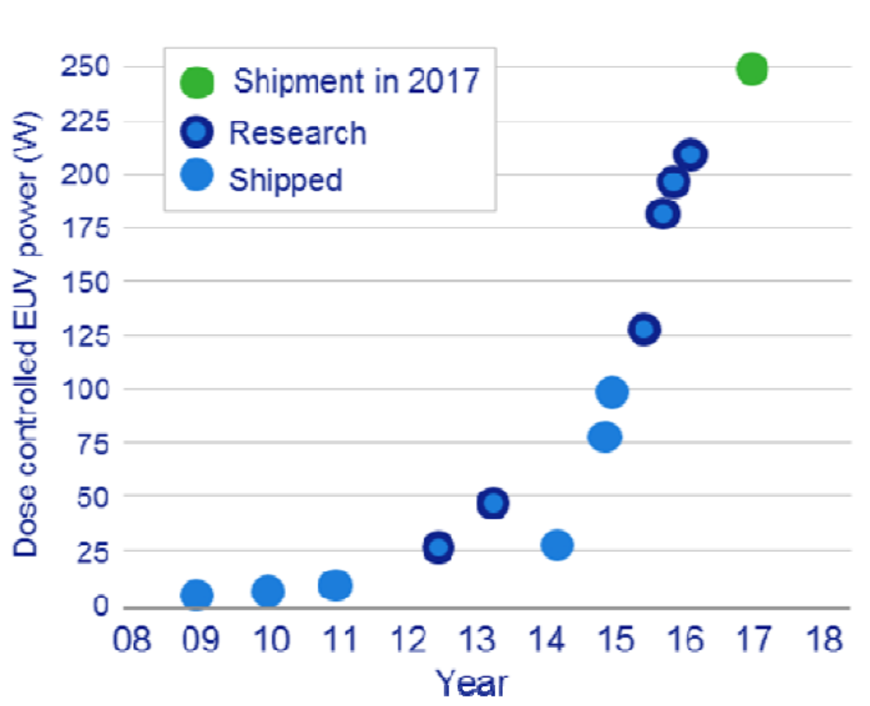
LE3=Litho+Etch+Litho+Etch+Litho+Etch

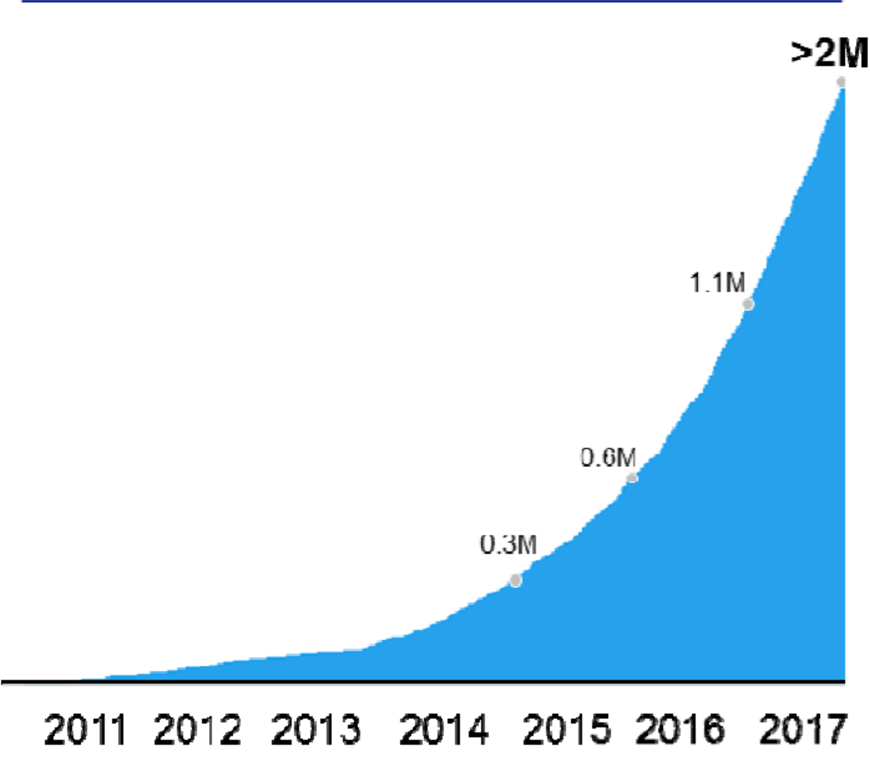
Source:http://staticwww.asml.com/doclib/investor/investor_day/asml_20161031_04_Investor_Day_2016_EUV_and_its_Business_Opportunity_HMeiling.pdf

ASML NXE:3400 System

Source: ASML Homepage, Image Library, https://www.asml.com/press/image-library/en/s44169

EUV Source Power





Source: Roderik van Es et al., "EUV for HVM: towards and industrialized scanner for HVM NXE3400B performance update," SPIE Advanced Lithography, 2018

High-NA projection optics

High-NA projection optics design available

Larger elements with tighter specifications

Source: J. van School et al., “High-NA EUV Lithography enabling Moore’s law in the next decade,” SPIE Photomask Technology + EUV Lithography, 2017

High-NA Surface Metrology

High-NA surface metrology

ZEISS

ASML

Public
Slide 35
EUVL 2017

- Accuracy of mirror surface metrology is key for imaging quality
- High-NA wave front needs 2x better measurement accuracy
- Larger mirrors: Diameter of mirrors about doubled

vacuum chambers

Courtesy Carl Zeiss SMT GmbH, 2016-09-20

Source: J. van School et al., “High-NA EUV Lithography enabling Moore’s law in the next decade,” SPIE Photomask Technology + EUV Lithography, 2017

“7 nm Technologies” in IEDM 2016

- IBM, GLOBALFOUNDRIES, and Samsung:
  - Poly Si (contacted): 44nm / 48 nm pitch （ArF-i）
  - Metal interconnect: 36nm pitch （EUV)
  - EUV lithography for Metal Interconnect
- TSMC:
  - SRAM cell size: 0.027 um^2
  - Poly Si (contacted): ?? nm pitch
  - Metal interconnect: ?? nm pitch
  - ArF immersion (ArF-i) lithography
    (R&D with EUV Lithography, too)

Ref: IEDM Technical Digest, 2016, Dec., 2016

IEDM 2016, #2.7 IBM/GF/Samsung

7nm MOL & BEOL Design Space Enabled by EUV

EUV

LE^n

2D

High-NA EUV

Layout

SADP

DSA

1D

SATP

SAQP

7nm FIN with SAQP

7nm Gate with SADP

50 40 30 20

Minimum pitch (nm)

Fig. 7. 7nm patterning approaches.

Source: R. Xie, et al, "A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels," IEDM Technical Digest, pp.47-50, pp, 2016

IEDM 2016, #2.7 IBM/GF/Samsung

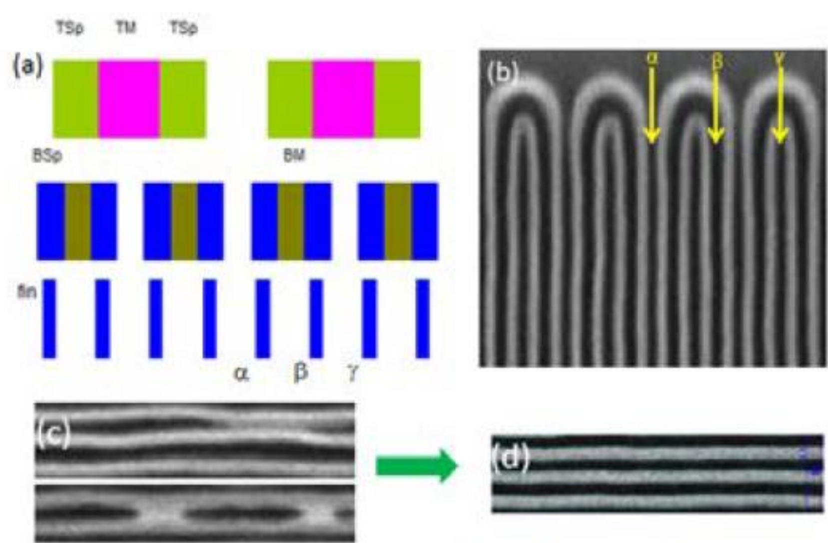


Fig. 8. (a) Schematic flow for self-aligned quadruple FIN patterning (SAQP); (b) Topdown SEM of the FINs formed with SAQP process. (c) un-optimized vs (d) Optimized SAQP process.

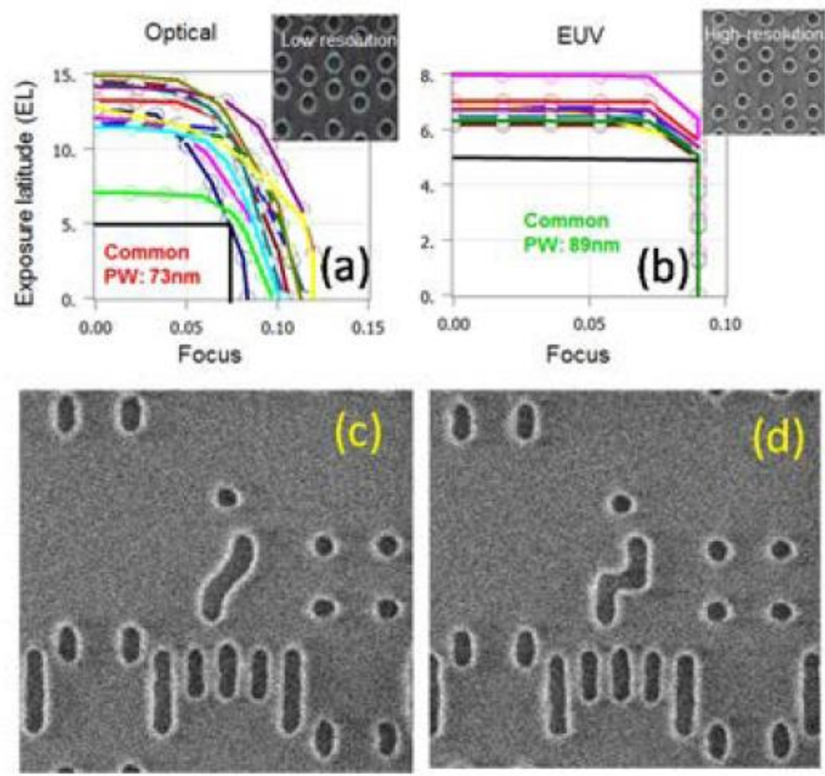


Fig. 12. (a)(b) Improved common process window in DOF and printing resolution achieved with EUV, compared to optical litho. (c)(d) Topdown SEMs of typical MOL EUV patterning with 45°, 90° cross-couple, respectively (24nm trench width).

Source: R. Xie, et al, "A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels," IEDM Technical Digest, pp.47-50, pp, 2016

EUV Infrastructure Readiness

EUV Infrastructure	11/14	10/15	11/15	10/16	02/17
E-beam mask inspection	[Green]	[Green]	[Green]	[Green]	[Green]
AIMS Mask Inspection	[Yellow]	[Yellow]	[Yellow]	[Green]	[Green]
Actinic Blank Inspection	[Yellow]	[Green]	[Green]	[Green]	[Green]
EUV Pellicle	[Yellow]	[Yellow]	[Yellow]	[Yellow]	[Yellow]
EUV Blank Quality	[Yellow]	[Yellow]	[Yellow]	[Yellow]	[Green]
Blank multi-layer deposition tool	[Red]	[Red]	[Yellow]	[Yellow]	[Green]
EUV Resist QC	[Red]	[Yellow]	[Yellow]	[Yellow]	[Green]
Actinic Patterned Mask Inspection	[Red]	[Red]	[Red]	[Red]	[Red]

Source: https://staticwww.asml.com/doclib/investor/presentations/2018/asml_20180314_2018-03-14_BAML_Taiwan_March_2018_FINAL.pdf

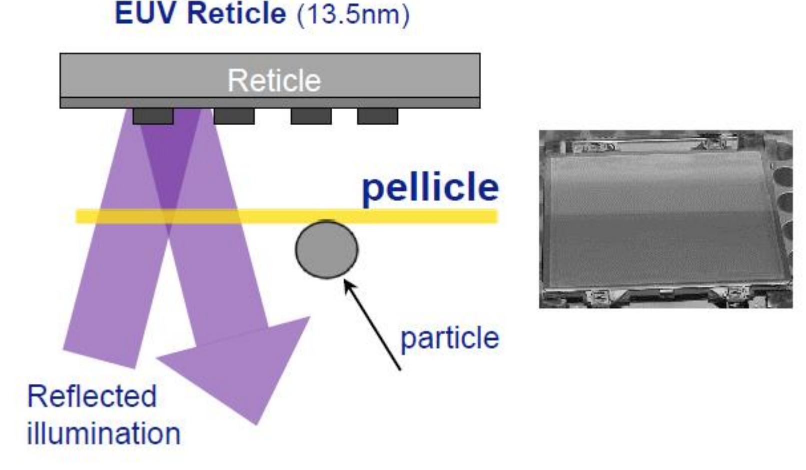
Reticle Front-Side Defects

Two-fold approach to eliminate reticle front-side defects

Public
Slide 10
2018 EUVL Workshop

1. Clean system
(without pellicle)

2. EUV pellicle



Source: A. Yen, "Continued Scaling in Semiconductor Manufacturing with EUV Lithography," 2018 EUVL Workshop, 2018

Defect Performance on EUV Scanners

adders per 10k wafers (52nm)

50

5

1

Scanner in-situ cleaning and hydrogen curtains provide >4x improvement

Flushing, parts cleanliness and reticle clamp improvements provide >2x improvement

POD, parts cleanliness and miscellaneous improvements ongoing to reach <1/10k

NXE3350B. 50/10k

NXE3400B: 3/10k

HVM

17H1

17H2

2018

Fig.9: Continuously improving defect performance roadmap on EUV scanners towards HVM requirements

Source: Roderik van Es et al., "EUV for HVM: towards and industrialized scanner for HVM NXE3400B performance update," SPIE Advanced Lithography, 2018

Pellicle for EUV Mask

Pellicle Film
EUV Transmission

83% transmission
Target 90%

Pellicle Mounting
Automated Equipment

ASML

Pellicle Performance
defects, Max Power

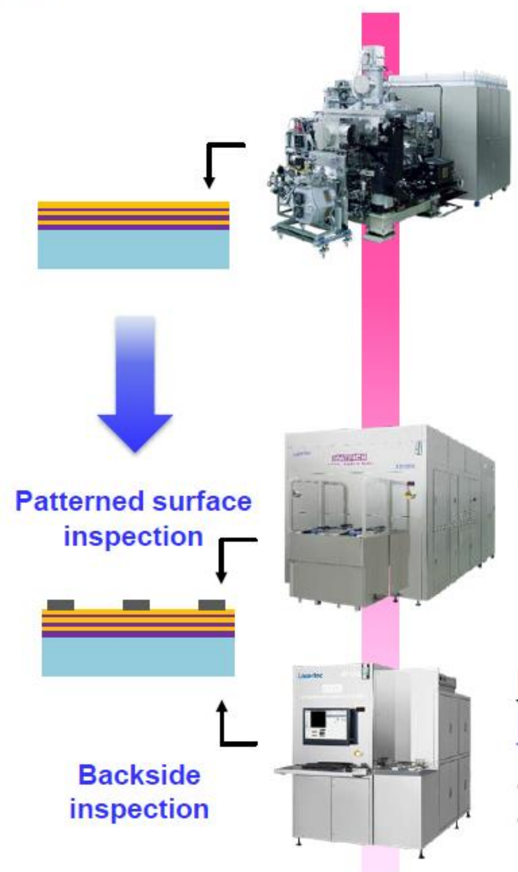
defects >10 micron
Max Power, W

>400
300
245
75
0
2016
2017
HVM
Target

Fig.10: The major pellicle improvements in the past year, 83% pellicle transmission (left), delivery to customers of automated pellicle mounting equipment (middle) and 0 defect pellicle performance (right)

Source: Roderik van Es et al., "EUV for HVM: towards and industrialized scanner for HVM NXE3400B performance update," SPIE Advanced Lithography, 2018

Lasertec's Mask Inspection Tools



Second Half of Fiscal Year 2018 - Goals and Actions
(2) Promotion of EUV-related Systems

EUV Mask Blanks Inspection System ABICS E120

- The system uses the wavelength of EUV lithography (13.5nm) for inspection
- The only system capable of detecting phase defects

Mask Inspection System
MATRICS X810 Series EUV Option

- Cutting-edge photomask inspection system
- Designed to inspect the patterned surface of EUV mask

EUV Mask Backside Inspection & Cleaning System
BASIC Series

- Designed for EUV mask backside inspection
- Capable of measuring the height of particles and cleaning them on the backside of EUV mask

16 Lasertec

Source: Lasertec Corporation, "First Half of Fiscal Year ending June 2018 Financial Results," Feb. 7, 2018
http://v4.eir-parts.net/DocumentTemp/20181018_015008987_djhaj255e3zsh0nchg2znof5_0.pdf

Stochastic Effects in EUV Lithography

	1. Save SEM images Total inspected area ≡ A	2. Image Processing STOCHALIS	
L/S		Microbridge	Broken Line
Contacts/Dots		“Missing” contact	“Bridging Contact

Source: P. De Bisshop and E. Hendrickx, “Stochastic effects in EUV lithography,” SPIE Advanced Lithography, 2018. Proc. SPIE 10583, Extreme Ultraviolet (EUV) Lithography IX, 105831K, doi: 10.1117/12.2300541

Stochastic Effects in EUV Lithography

Line/Space

Post-etch

P36

Bridging

Breaking

1E-3
1E-4
1E-5
1E-6
1E-7

pixNOK

inspected area ~150 μm²

5429_S06E

detection limit

13 14 15 16 17 18 19 20 21

Mean Space CD [nm]

Contacts

Post-litho

P40x40

Missing

Bridging

0.1
0.01
1E-3
1E-4

NOK Contacts

3792_S17

detection limit

15 16 17 18 19 20 21 22 23 24 25 26 27

Mean CD [nm]

Source: P. De Bisshop and E. Hendrickx, "Stochastic effects in EUV lithography," SPIE Advanced Lithography, 2018. Proc. SPIE 10583, Extreme Ultraviolet (EUV) Lithography IX, 105831K, doi: 10.1117/12.2300541

EUV-FEL (Free Electron Laser)

Achieved values in cERL and Design values at the EUV-FEL

Items	Achieved values in cERL	Design Values at the EUV-FEL
Energy for injector (MeV)	2.9-6	10.5
Energy of Accelerator(MeV)	20	800
Charge /bunch (pC)	0.7-5	60
Repetition rate (MHz)	162.5-1300	162.5
Average Current (mA)	1.0	9.75
Emitance for electron beam (mm mrad)	0.3-1	0.6
Gradient of the accelerated energy (MV/m)	8.6	12.5
Wavelength of EUV-FEL (nm)	/	13.5
Average power of EUV-FEL (kW)	/	Higher than 10 kW

cERL in KEK

1st Arc
Chicane
Beam Dump
~200 m
Undulators(FEL)
Main Linac
High Power EUV-FEL Light
Injector Diagnostic Line
Merger
Injector Linac
2nd Arc
~20 m
Gun

Fig. 2 Prototype design of the EUV-FEL

Source: H. Kawata, “Strategy to realize the EUV-FEL high power light source,” 2016 International Symposium on Extreme Ultraviolet Lithography, Hiroshima, Japan, Oct. 24, 2016

Key Challenges

Key Challenges 2019

- Materials :
  - some new suppliers (Zeon, PiBond, IM)
  - Inpria scaling
  - Defects/stochastic performance still a concern. Will 3400 solve this ? (comparison)
- Source
  - 250W or 500W ? first consistency needed
  - 1000 wafers per day (not at 250W), 140 wph
- Masks :
  - Good progress on actinic PMI
  - Pellicle still a major challenge
  - Alternative absorber key for extendibility

- End customers : no presentation or not attending
- Resist vendors work with their customers and are not allowed to share results

Input from 16th International EUVL Symposium Steering Committee. Monterey, CA, September 20, 2018

EUV Focus Areas

EUVL insertion for 2019 : optimism

Short term development	Average	StdDev
1. Multiple EUV materials capable for insertion	2.29	1.26
2. NXE3400 with 250W in the field now at >80% availability	2.64	1.27
3. Insertion happening without pellicle	2.71	0.96
4. Actinic mask making tools going into production	3.64	0.84

Ranked by 16th International EUVL Symposium Steering Committee. Monterey, CA, September 20, 2018

Source: "Closing Address,"SPIE Photomask Technology + EUV Lithography 2018, Monterey, U.S.A., Sept. 20, 2018

EUV Focus Areas

EUVL extension challenges

Long term development concerns	Average	StdDev
1. Resist resolution, stochastics, and sensitivity met simultaneously	1.28	0.82
2. Keeping mask defect free (pellicle, or other...)	2.57	0.85
3. Reliable source >250W operation with >90% availability	2.71	0.99
4. Continue actinic PMI and new mask material development	3.43	0.5

Ranked by 16th International EUVL Symposium Steering Committee. Monterey, CA, September 20, 2018

Source: "Closing Address,"SPIE Photomask Technology + EUV Lithography 2018, Monterey, U.S.A., Sept. 20, 2018

EUV Focus Areas

EUVL insertion for 2019 is happening

2014	2015	2016	2017	2018
1.Reliable source operation with > 75% availability	1.Reliable source operation with > 85% availability	1.Reliable source operation with >85% availability	1.Reliable source >250W operation with >90% availability	1. Multiple EUV materials capable for insertion
2.Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, stochastics, and sensitivity met simultaneously	2. NXE3400 with 250W in the field now at >80% availability
3.Mask yield & defect inspection/review infrastructure	3. Mask yield & defect inspection/review infrastructure	3. Keeping mask defect free	3. Keeping mask defect free	3. Insertion happening without pellicle
3. Keeping mask defect free	4. Keeping mask defect free	4. Mask yield & defect inspection/review infrastructure	4. Mask yield & defect inspection/review infrastructure	4. Actinic mask making tools going into production

imec EUREKA EIDEC SPIE.

Source: “Closing Address,”SPIE Photomask Technology + EUV Lithography 2018, Monterey, U.S.A., Sept. 20, 2018

EUV Focus Areas

EUVL extension challenges

2014	2015	2016	2017	2018
1.Reliable source operation with >75% availability	1.Reliable source operation with > 85% availability	1.Reliable source operation with > 85% availability	1. Resist resolution, stochastics, and sensitivity met simultaneously	1. Resist resolution, stochastics, and sensitivity met simultaneously
2.Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Reliable source >250W operation with >90% availability	2. Keeping mask defect free (pellicle, or other...)
3.Mask yield & defect inspection/review infrastructure	3. Mask yield & defect inspection/review infrastructure	3. Keeping mask defect free	3. Keeping mask defect free	3. Reliable source >250W operation with >90% availability
3. Keeping mask defect free	4. Keeping mask defect free	4. Mask yield & defect inspection/review infrastructure	4. Mask yield & defect inspection/review infrastructure	4. Continue actinic PMI and new mask material development

Source: "Closing Address,"SPIE Photomask Technology + EUV Lithography 2018, Monterey, U.S.A., Sept. 20, 2018

Mass production with EUV

Industry Shrink Roadmap & EUV insertion

ASML
Public
Slide 23
October 31, 2016

EUV Production Insertion Window

HVM	2014	2015	2016	2017	2018	2019	2020	2021	2022

Customer comments on EUV insertion (see next slide)

When

Logic — Node name: 20nm, 16/14nm, 10nm, 7nm, 5nm, 3nm

Performance Memory — DRAM — Minimum half pitch: 28-30, 20-22, 1X, 1Y, 1Z, next

Storage Class Memory — PC-RAM, ReRAM, X-point etc. — Minimum half pitch /x number of layers: 2X'/x2, 1X"/x4, 1Y"/x8, 1Z"/x8

Storage Memory
- Planar Floating Gate NAND: 22, 17-18, 14-15
- 3D NAND — x number of layers: x24, x32, x48, x64, >x96, >x128, >x192, >x200

Today's status
- Production[1]
- Development[1]
- Research[1]
- Roadmap[2]

Source: 1) Customers - public statements,, IC Knowledge LLC; 2) ASML extrapolations

Source:http://staticwww.asml.com/doclib/investor/investor_day/asml_20161031_04_Investor_Day_2016_EUV_and_its_Business_Opportunity_HMeiling.pdf

Mass Production with EUV: TSMC

TSMC to Start 5nm Production in April

5 October 2018

SAN JOSE, Calif. — TSMC taped out its first chip in a process making limited use of extreme ultraviolet lithography and will start risk production in April on a 5-nm node with full EUV.

…

In process technology, TSMC announced that it taped out a customer chip in an N7+ node that can use EUV on up to four layers. Its N5 that will use EUV on up to 14 layers will be ready for risk production in April. EUV aims to lower costs by reducing the number of masks required for leading-edge designs.

Source: EE Times Asia
https://www.eetasia.com/news/article/18100502-tsmc-to-start-5nm-production-in-april

- 2019年4月にEUVによる5nm世代のリスク生産を開始
- N7+世代ではEUVを4層まで利用可
- N5世代ではEUVを14層まで利用可

Mass Production with EUV: Samsung

Samsung Ramps 7nm EUV Chips

17 October 2018

SAN JOSE, Calif. — The race is on to get the first chip made with extreme ultraviolet lithography out the foundry door.

Samsung said it has taped out and is ramping multiple 7nm chips using EUV following a similar announcement earlier this month from its larger foundry rival TSMC.

…

In its core memory business, Samsung said that it is sampling 256-GByte RDIMMs made with its 16-Gbit chips.

…

The chips are made in a 1y-nm process first described a year ago. It was not clear whether EUV is being applied to the 1y process. However, follow-on 1z and 1a nodes will increasingly use EUV, suggested Samsung's head of DRAM development, Seong Jin Jang, in a talk here.

Source: EE Times
https://www.eetimes.com/document.asp?doc_id=1333881

- EUVを使って複数の7nm（ロジック）チップの量産開始
- 1y世代の16Gbit DRAMチップによる256GByte RDIMM*をサンプリング中。この世代でEUVが使われているかどうかはわからない
- 1zと1a世代のDRAMではEUVの利用が増えると発言

* RDIMM: registered dual in-line memory moduleの略。Registered Bufferを内臓したメモリモジュール。サーバなどで使われる。

Summary

- EUV source power of 250W has been achieved.
- Key challenges in EUV Lithography are pellicle, actinic pattern inspection, stochastics, etc.
- EUV lithography will be used in mass production tool for 7nm or 5nm logic products and beyond.
- EUV-FEL is a possible solution as an EUV source with higher average power than 1 kW. Its cost of ownership, peak power, coherence of the EUV-FEL source might be the potential problems to be solved

Glossary

CD: Critical Dimension
DP: Double Patterning
DSA: Directed Self Assembly
EUVL: Extreme Ultraviolet Lithography
LER: Line Edge Roughness
LWR: Line Width Roughness
ML: Maskless Lithography
NA: Numerical Aperture
IRDS: International Roadmap for Devices and Systems
ITRS: International Technology Roadmap for Semiconductors
SADP: Self Aligned Double Patterning
SAQP: Self Aligned Quadruple Patterning
QP: Quadruple Patterning
SP: Quadruple Patterning