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Observation of lattice undulation of commercial bonded silicon-on-insulator wafers by synchrotron X-ray topography

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Introduction

The application of silicon-on-insulator (SOI) technology to low-power and high-speed LSIs is becoming widespread. This is based on the significant progress being made in wafer manufacturing processes. In the case of bonded SOI wafers, two kinds of sophisticated techniques have been developed: one is made by transfer of an epitaxial layer over porous Si[1], and the other is processed using hydrogen-delamination-induced splitting[2]. They have markedly improved the crystalline quality and the thickness uniformity of the SOI layers. For conventional bonded SOI wafers of which the SOI layers were thinned by conventional lapping and polishing, Matsui et al. showed by using a synchrotron X-ray microbeam technique that the lattice plane of the SOI layers undulated at the tilt angle of more than 16 arc seconds with the typical spatial interval ranged from 10 to 100 mm[3]. Similar lattice distortion of an SOI layer was also observed by X-ray topography studies[4]. It is therefore important to investigate if such lattice distortion exists in the sophisticated commercial bonded SOI wafers.

In this paper, we show X-ray topographs of two kinds of the sophisticated bonded SOI wafers, using synchrotron radiation (SR), which enabled us to obtain X-ray images from SOI layers of 100 nm thickness.

Experimental

Three commercial [001]-oriented SOI wafers were prepared in this study. Two of them (A1 and A2) were made by a method proposed by Yonehara et al.[1], in which an epitaxial Si layer over porous Si is transferred onto a substrate and subsequently split at the porous Si layer by water jet. Sample A1 had a 2000-nm-thick SOI layer and a 200-nm-thick buried oxide (BOX) layer. The as-received wafer was set on a sample holder of a precision goniometer and X-ray topographs were taken from the vicinity of the center of the wafer. The SOI and BOX layers of Sample A2 were each 100 nm thick. A rectangular sample of 20×10 mm^2 size was cut out from the wafer. Tired sample (B1) was processed using hydrogen-delamination-induced splitting[2]. The SOI and BOX layers of Sample B1 were 100 nm and 200 nm thick, respectively.

Synchrotron X-ray topography experiments were carried out at the BL-15C of Photon Factory, KEK, Tsukuba, Japan. The 220 reflection in Laue case and the asymmetric 115 reflection in Bragg case with a glancing angle of 4.1 degrees were used. The X-ray film used was Fuji IX-100. The SR beam was monochromatized to 17.4keV using a Si (111) double-crystal monochromator and a square beam of 2×2 mm2 size formed by a four-quadrant slit was irradiated onto the sample from the SOI layer.

Results

As there exists an unintentional misorientation between the SOI layer and the substrate of bonded SOI wafers, the topographic image of the SOI layer could be separated from that of the substrate. Fig.1 shows typical topographs of the SOI layer and the substrate of Sample A1 taken with the 220 reflection in Laue case. The topograph of the substrate shows a uniform zonal image due to a warpage of a few arc seconds caused by sample holding. On the other hand, the topograph of the SOI layer exhibits a wrinkled pattern with the ruffled contrast of an interval of dozens of micrometers. Such a wrinkled pattern was seen everywhere on the SOI.

References

[1] T. Yonehara, K. Sakaguti and N. Sato: Appl. Phys. Lett. 64, 2108 (1994).
[2] M. Bruel, B. Aspar and A. J. Auberton-Hervé: Jpn. J. Apple. Phys 36, 1636 (1997).

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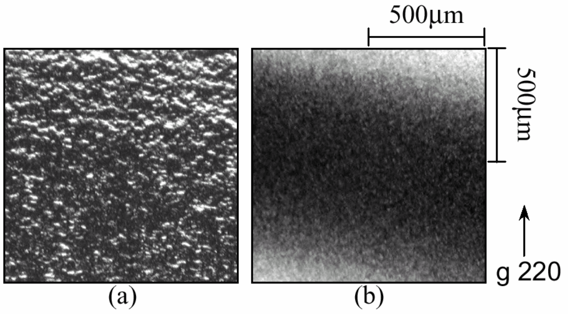

Fig.1 X-ray topographs of Sample A1 with the SOI layer of 2000 nm thickness, (a) for the SOI layer and (b) for the substrate.