

Characterization of SiC Crystals and Devices for Power-Electronics Inverter by means of X-ray topography

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Power electronics is a technology concerned with the processing of electrical power with high efficiency. It is used in a variety of fields; electric appliance, transportation using electric power such as motor vehicle and railroad, control in electric-power supply and distribution, *etc.* Prospective increase in use of electric power requires expansion in capacity, improvement in efficiency and downsizing for the future power-electronic device units. The performance of the power-electronic device made with silicon (Si) is, however, approaching the limits due to the material parameters. Alternatively, silicon carbide (SiC) is a promising material to overcome the Si limits, and the SiC technology is now being developed extensively toward the practical application.

We have characterized defects in SiC crystal and device by means of X-ray topography at BL15C in the research project for three years (FY 2006-2008). Test element groups (TEGs) were prepared, and origins of device failure were investigated using defect mapping by electron-beam-induced current (EBIC) measurement and emission microscopy as well as X-ray topography.

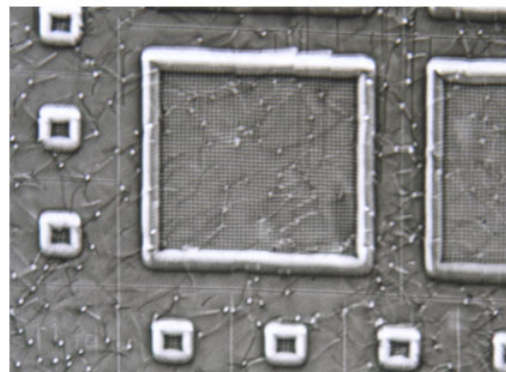
We developed a special goniometer for the study. The goniometer was equipped with azimuthal rotation (ϕ) and tilt axes (ψ) in addition to precision ω and 2θ axes. The stage on the ϕ -axis was designed so that diffraction topographs could be taken in both Laue and Bragg cases. The ϕ -stage was equipped on the two-dimensional translation stage to focus on any places of the wafer up to 4 inches in diameter. The diffraction condition was adjusted by monitoring diffraction image using the flat-panel sensor (HAMAMATSU C9732DK), and the topograph was recorded on a nuclear emulsion plate (Ilford L4).

X-ray topography experiments were performed mainly in the Bragg-case (reflection) geometry. Since devices were fabricated on a top surface of wafer, the Bragg-case geometry was useful to observe dislocations in the device layer[1]. Several TEGs were fabricated on 2-inch wafers, which were pn-junctions to simulate MOSFET with special structures, for example, and their voltage-current characteristics and reliability were studied. The issue was whether the dislocations induced device failure and degradation. There observed some positional correlations between dislocation and device failure. Threading screw

dislocation was an example showing current-leakage under reverse-biased conditions. The leakage was, however, found in not all of screw-dislocations. This fact indicates that dislocation is not the only reason to induce failures.

We have speculated that impurity atoms are involved with dislocation-related troubles [2]. X-ray fluorescence spectroscopy was performed at BL4A in order to distinguish impurity metal elements concentrating locally on dislocations. Some metal elements were detected from wafers, but their effect on the device performance is still an open question.

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0.5mm

Fig. 1 An example of X-ray topograph of SiC device.

References

- [1] T. Ohno et al., *J. Cryst. Growth* **260**, 209 (2004).
- [2] T. Ohyanagi *et al.*, *Materials Science Forum* **615-617**, 707 (2009).